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Study Of Design For Reliability Of Rf And Analog Circuits

Hongxia Tang
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STUDY OF DESIGN FOR RELIABILITY OF RF AND ANALOG CIRCUITS

by

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M.S. University of Central Florida, 2007

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for the degree of Doctor of Philosophy
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ABSTRACT

Due to continued device dimensions scaling, CMOS transistors in the nanometer regime have resulted in major reliability and variability challenges. Reliability issues such as channel hot electron injection, gate dielectric breakdown, and negative bias temperature instability (NBTI) need to be accounted for in the design of robust RF circuits. In addition, process variations in the nanoscale CMOS transistors are another major concern in today's circuits design.

An adaptive gate-source biasing scheme to improve the RF circuit reliability is presented in this work. The adaptive method automatically adjusts the gate-source voltage to compensate the reduction in drain current subjected to various device reliability mechanisms. A class-AB RF power amplifier shows that the use of a source resistance makes the power-added efficiency robust against threshold voltage and mobility variations, while the use of a source inductance is more reliable for the input third-order intercept point.

A RF power amplifier with adaptive gate biasing is proposed to improve the circuit device reliability degradation and process variation. The performances of the power amplifier with adaptive gate biasing are compared with those of the power amplifier without adaptive gate biasing technique. The adaptive gate biasing makes the power amplifier more resilient to process variations as well as the device aging such as mobility and threshold voltage degradation.

Injection locked voltage-controlled oscillators (VCOs) have been examined. The VCOs are implemented using TSMC 0.18 μm mixed-signal CMOS technology. The injection locked oscillators have improved phase noise performance than free running oscillators.

A differential Clapp-VCO has been designed and fabricated for the evaluation of hot electron reliability. The differential Clapp-VCO is formed using cross-coupled nMOS transistors, on-chip transformers/inductors, and voltage-controlled capacitors. The experimental data demonstrate that the hot carrier damage increases the oscillation frequency and degrades the phase noise of Clapp-VCO.

A p-channel transistor only VCO has been designed for low phase noise. The simulation results show that the phase noise degrades after NBTI stress at elevated temperature. This is due to increased interface states after NBTI stress. The process variability has also been evaluated.

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LIST OF ACRONYMS/ABBREVIATIONS

DFR	Design for Reliability
HCE	Hot Carrier Effect
HBD	Hard Breakdown
IIP3	Input Third-order Intercept Point
LER	Line Edge Roughness
LNA	Low Noise Amplifier
LWR	Line Width Roughness
NBTI	Negative Bias Temperature Instability
OTV	Oxide Thickness Variation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PA	Power Amplifier
PAE	Power Added Efficiency
RDF	Random Dopant Fluctuations
RF	Radio Frequency
ILO	Injection Locked Oscillator
SBD	Soft Breakdown
TDDB	Time Dependent Dielectric Breakdown
VCO	Voltage Controlled Oscillator

CHAPTER 1 : INTRODUCTION

1.1 Motivation

With the continued scaling of modern CMOS technology, radio-frequency (RF) circuits have been widely implemented in CMOS technology due to its cost advantage, high integration capability and improving high frequency performance. The state-of-the-art CMOS technology is attractive for RF circuit design for system-on-a-chip applications in which digital baseband, mixed-signal, and RF transceiver blocks are integrated on a single die. Many analog/RF blocks in wireless transceiver/receiver such as low noise amplifier (LNA), mixer, power amplifier and voltage-controller oscillator (VCO) have been successfully implemented in CMOS technology nowadays. The cut-off frequency (f_T) and maximum frequency (f_{max}) have been reported above 300 GHz at room temperature [1]. Integrated RF circuits in CMOS operating at 100 GHz and beyond have already been reported [2-3].

Due to continued scaling device dimensions, CMOS transistors in the nanometer regime have resulted in major reliability and variability challenges. The smaller feature size makes the CMOS device more sensitive to the process variations and stress induced degradations. For the radio frequency circuits using these CMOS devices, significant performance degradation can be induced from the degradation of single transistor. Thus RF circuit design needs account for the device reliability effects from gate dielectric breakdown [4]-[7], hot carrier effect [7]-[10], and bias temperature instability [11]-[13]. In addition, process variations due to random dopant fluctuation, oxide thickness variation and line edge roughness are another major concern in today's circuit design with advanced CMOS technology [14]-[18].

The circuit design for reliability (DFR) is becoming increasingly important for nanoscale electronics [19]. In practical IC development, it's essential to add a reliability simulation and analysis phase before circuit fabrication. To improve the product yield and to meet the reliability requirements, designers normally provide relatively large design margin. Good understand in DFR means a reduction of over-design to improve additional circuit performances while maintaining required reliability. The ultimate goal of DFR is to design reliable electronics that are capable of postprocess adjustment and whose performances insensitive to the transistor parametric drift after stress over time [20]. Recently, numerous papers on reliability for digital and mixed signal circuits were published [21]-[23].

In this work, the adaptive gate-source biasing and adaptive gate biasing schemes are proposed for the RF power design for circuit reliability and process variability. Direct Injection locked and tail injection locked oscillators are examined to lower phase noise of oscillators. A differential Clapp-VCO is designed and implemented to examine the hot carrier effect. And the reliability and variability of a p-channel transistor only VCO is discussed.

1.2 Organization

Chapter 2 gives an introduction to the major reliability and variability issues on the Modern MOSFETs device. It presents the degradation mechanisms of hot carrier effect (HCE), oxide breakdown, negative temperature bias instability (NBTI) and their effects on MOSFETs parameters. It also presents the variability issues due to process variations.

Chapter 3 presents an adaptive gate-source biasing scheme to improve the RF circuit reliability. The adaptive method automatically adjusts the gate-source voltage to compensate the

reduction in drain current subjected to various device reliability mechanisms. A class-AB RF power amplifier shows that the use of a source resistance makes the power-added efficiency robust against threshold voltage and mobility variations, while the use of a source inductance is more reliable for the input third-order intercept point.

Chapter 4 presents the reliability and variability improvement using gate biasing for CMOS RF power amplifier. The simulation results demonstrate that the power gain, power-added efficiency have less variation for stress induced threshold and mobility degradation and process variability for the gate biased power amplifier.

Chapter 5 reviews the principle of oscillator and injection locking. The two port feedback model and one port negative resistance model used to describe oscillators are introduced. The model and characteristic of VCO is reviewed. The concept of injection locking is also described in this chapter.

Chapter 6 examines two injection locking voltage-controlled oscillators (VCOs)-direct injection oscillator and tail injection oscillator. The oscillators are implemented with standard 0.18 μ m technology and work around 2.4GHz. The injection locked oscillators have improved phase noise performance than the free running oscillators.

In chapter 7 a differential Clapp-VCO has been designed and fabricated for the evaluation of hot electron reliability. The differential Clapp-VCO is formed using two single ended nMOS-cores, a cross-coupled nMOS pair and a transformer. The experimental data indicate that the hot carrier damage increases the oscillation frequency and degrades the phase noise of Clapp - oscillator.

Chapter 8 investigates the process variability of a cross-coupled LC VCO. The VCO is designed using a cross-coupled pMOS pair to get better phase noise performance. The simulation result shows that the phase noise degrades at elevated temperature. And the increased interface states caused by NBTI effect also results in the phase noise degradation. The process variability has been evaluated for the performance of the VCO.

Finally, a summary of this dissertation is given in chapter 9.

CHAPTER 2 : DEVICE RELIABILITY AND VIARIABILITY

2.1 Introduction

Over the past three decades, the CMOS technology has been continuing scaling down for improving speed and functionality [24][25]. The aggressive scaling in device dimensions results in major reliability issues for CMOS transistors such as hot carrier effect, time dependent dielectric breakdown (TDDB) and negative bias temperature instability (NBTI). The transistors suffer from hot carrier effect due to high electric field and impact ionization at the drain region for short-channel MOSFETs [26][27]. Hot electron effect could increase the threshold voltage and decrease the transconductance of MOSFETs. Hot electron effect could also result in RF circuit parameters degradation such as noise figure, phase noise, power efficiency etc [8][28][29]. Time-dependent dielectric breakdown could be induced due to the high electric field across the gate insulator for ultra-thin gate oxide of transistors [30][31]. The threshold voltage and mobility of the transistors are degraded after soft breakdown [6]. Besides, negative bias temperature instability due to the buildup of positive charges and surface states in the gate oxide leads to an increase of threshold voltage and decrease of the drive current [12].

The continuous scaling of CMOS technology also increases the concern of the CMOS process variability [32][33]. The process-variability induced device performance variation becomes a critical issue in the circuit design with the advanced CMOS technology [34]. Process variation has significant impact on the performance of SRAM and logic circuits [35], inverter delays [36], and analog circuits [37]. The major sources of process variability include random

dopant fluctuations (RDF), line-edge and line-width roughness (LER and LWR) and oxide thickness and interface roughness etc [38].

2.2 Transistor Reliability Issues

2.2.1 Hot Carrier Effect

Hot carrier effect is one of the most significant reliability problems of advanced MOSFETs devices. Hot carriers are electrons or holes obtained very high kinetic energy accelerated by high electric field. These energetic carriers injected into the gate dielectric where they get trapped or generate interface states. These defects then lead to threshold voltage shifts and transconductance degradation of MOS devices.

There are four kinds of hot carrier injection mechanisms: drain avalanche hot-carrier (DAHC) injection, channel hot-electron (CHE) injection, substrate hot-electron (SHE) injection and secondary generated hot-electron (SGHE) injection [39].

The drain avalanche hot carrier occurs when the drain voltage is high and the gate voltage is lower than the drain voltage. At this condition, the electric field near the drain region is very high. The channel carriers are accelerated by the high electric field and get enough energy to cause impact ionization. The electron and hole pairs generated by avalanche multiplication are also accelerated by the electric field. Some electrons with enough energy to surmount the Si-SiO₂ barrier are injected into gate oxide. The injected hot carriers could be trapped at the Si-SiO₂ interface or trapped in the gate oxide causing threshold voltage shift or transconductance reduction. Most of the generated holes flow back to substrate increasing the substrate leakage

current. The mechanism of drain avalanche hot carrier injection is shown in Fig. 2.1 (a). It's reported that the worst effects occurs when the gate voltage is half of the drain voltage $V_G = \frac{1}{2} V_D$.

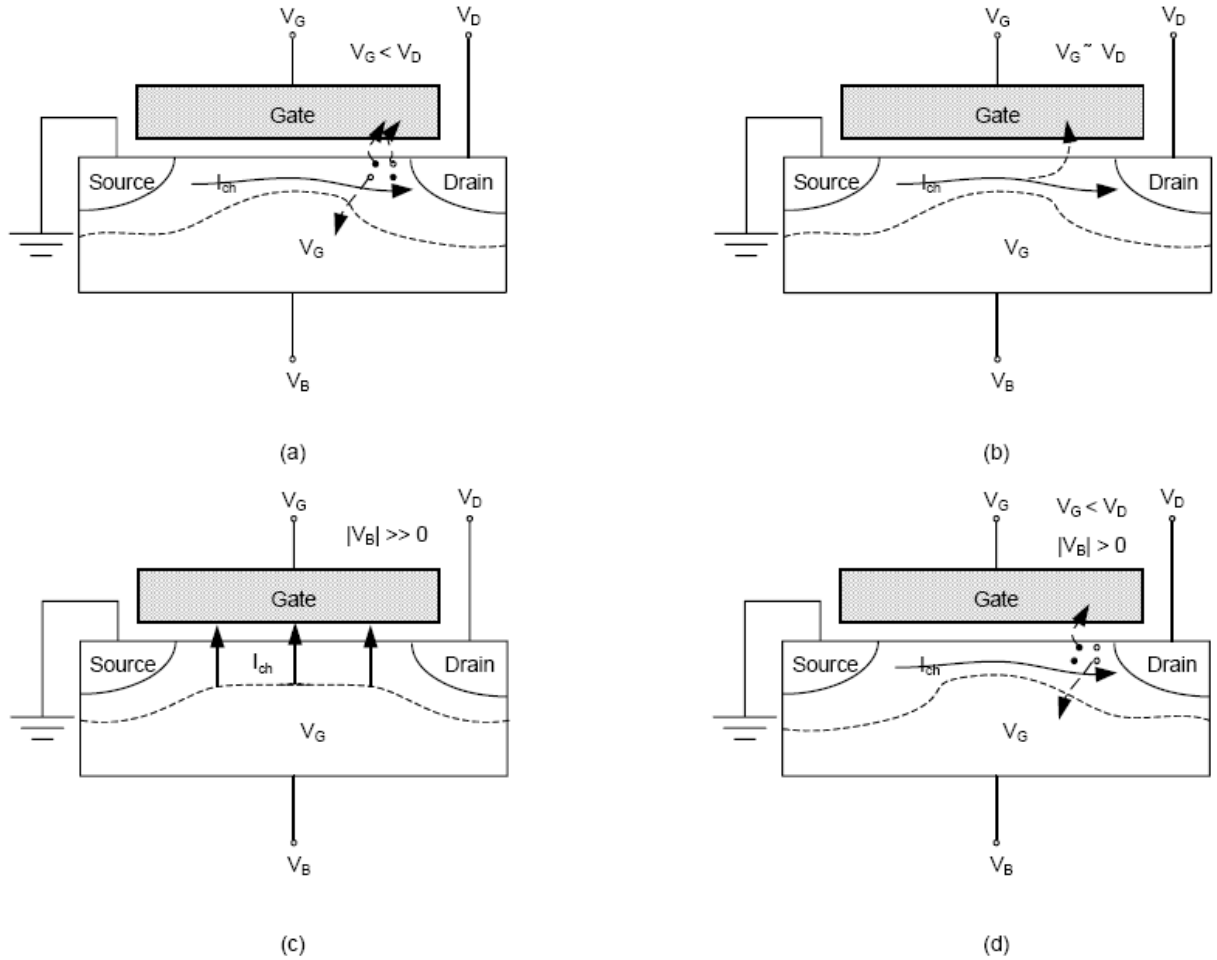


Figure 2.1 Hot carrier effect mechanisms (a) drain avalanche hot carrier injection (b) channel hot-electron injection (c) substrate hot-electron injection (d) secondary generated hot-electron injection

The Channel hot-electron injection occurs at the gate voltage is approximately equal to the drain voltage $V_G \approx V_D$. Some “luck electrons” get enough energy along the channel and are attracted by the high gate voltage to inject into the gate oxide. The injected carriers cause

interface and oxide degradation and increase gate leakage current. The mechanism of channel hot-electron injection is shown in Fig. 2.1 (b).

When there is a positive or negative voltage applied to the backside of the substrate, the substrate hot-electron or hot-hole will happen. The carriers in the substrate are driven by the substrate field toward the Si-SiO₂ interface. The carriers then get further kinetic energy in the surface depletion region and are injected into the gate oxide. The process of substrate hot-electron injection is shown as in Fig. 2.1 (c).

For secondary generated hot-electron injection, a photon generated electron-hole pairs have secondary impact ionization by the high electric field near the drain. Besides the voltage is high and $V_G < V_D$, there is also an additional voltage applied to the backside of the substrate. The secondary impact ionized carriers driven to the Si-SiO₂ surface by the substrate field and accelerated further by the high electric field in the drain region can inject into the gate dielectric causing degradation. The process is shown as in Fig. 2.1 (d).

With the scaling of the MOSFET technology, the hot electron effect is getting more significant due the shorter channel length and thinner gate dielectric. The hot electron stress will induce the threshold voltage shifting and the mobility degradation due to the generation of traps in the gate dielectric and interface states at the silicon and silicon dioxide interface [40][41].

2.2.2 Time Dependent Dielectric Breakdown

Gate dielectric provides insulation of the gate electrode from the conducting channel for transistors. The gate dielectric reliability is very important for the device reliability. The breakdown happens when the insulation property of the silicon dioxide in the CMOS gate is

destroyed by the formation of a conducting path through the oxide and the substrate. As the technology scaling down, the thickness of the gate dielectric also scaling down with the technology. Thus, the gate dielectric is getting more vulnerable to the electric field across the gate and the time dependent dielectric breakdown is becoming more severe.

The gate dielectric breakdown is considered due to a combination of several mechanisms: charge injection, trap state generation, and trap-assisted conduction [25]. The process of dielectric breakdown could be described with a percolation theory [42]. At the beginning of operation, traps start to form in the gate oxide. But they don't overlap and conduct. The leakage current is enhanced through various hopping and tunneling processes. As more and more traps are created, the traps overlap with each other and form a conduction path. The soft breakdown (SB) happens once the conduction path is created. The soft breakdown will not cause failure of device, but it will increase the transistor gate leakage current and degrade the threshold voltage and mobility. The soft breakdown will also result in variation of circuit performance [43][44]. The conduction of soft breakdown then leads to thermal damage and creates more trap states. With accumulative traps and conduction, the gate oxide is punched through and the hard breakdown (HBD) happens. HBD is a catastrophic failure of the device and hence the entire circuit. When the dielectric is getting thinner, breakdown is more easily to happen since the fewer traps are needed to cause BD.

2.2.3 Negative Bias Temperature Instability

One of the temperature related reliability issues for MOSFETs is the bias temperature instability (BTI). Under normal operation condition, BTI is only significant for PMOS transistors

with negative gate bias. Negative bias temperature instability (NBTI) for PMOS transistors is a major reliability concern for advanced CMOS technology.

The mechanism for NBTI can be explained by the reaction-diffusion (RD) model [45]. Under a constant gate voltage and an elevated temperature, the holes in the inversion layer of PMOS transistors react with the Hydrogen terminated trivalent Si bonds (Si-H) at the Si-SiO₂ surface. The dissociation of the Si-H bonds generates positively charged interface state Si⁺. The released hydrogenated species (H⁺) diffuse away from the interface toward the polysilicon gate and are trapped near the oxide interface producing the positive oxide charges (Si-OH⁺-Si). The buildup of positive charges at the Si-SiO₂ interface or in the oxide layer causes the PMOS performances degradation.

NBTI will result in threshold voltage shift of PMOS due to the interface states and traps. The threshold voltage shift ΔV_T by negative bias temperature stress follows a power law relationship with time [46]. It's reported that the NBTI effect for AC stress is smaller than DC stress [47] which may be due to interface trap annealing and holes detrapping during the off phase of the stress waveform. PMOS transistors experiencing NBTI stress are also subjected to mobility degradation [48].

2.3 Process Variability

The major sources of process variability include random dopant fluctuations (RDF), line-edge and line-width roughness (LER and LWR) and oxide thickness and interface roughness etc [38].

Random dopant fluctuations results from the random fluctuations in the number and location of the dopant atoms in the channel of a transistor and is a major source of process variability in advanced CMOS technology. As the number of dopant atoms in the channel decreases with scaled dimensions, the impact of the variation associated with the atoms increases. The major effect of random dopant fluctuations is introducing threshold voltage shift and mismatch. The impact of process variability due to dopant variation on threshold voltage mismatch derived from the overall number variation of the total depletion charge is given by [49][50]:

$$\delta V_T = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{si} \phi_B}}{2} \right) \frac{T_{ox}}{\varepsilon_{ox}} \left(\frac{\sqrt[4]{N_{CH}}}{\sqrt{W_{eff} L_{eff}}} \right) \quad (2.1)$$

where q is the electron charge, ε_{si} , ε_{ox} are the permittivity of the silicon and SiO_2 , ϕ_B is the built-in potential of S/D-to-channel PN junction of MOFETs, N_{CH} is the channel doping concentration, L_{eff} is the effective channel length and W_{eff} is the effective channel width. The threshold voltage variation is inversely proportional to the square root of the active device area. As a result of scaling down technology, dopant variation is significantly increased in the process variability for scaled CMOS technology beyond 90-nm regime. As an example, it is estimated that the random dopant fluctuation contributes over 60% to the threshold voltage mismatch in sub-90-nm MOSFETs [33].

The second major source of process variability is line-edge and line-width roughness that causes the critical dimension variation and is due to the tolerances inherent to materials and tools used in the lithography process. The edge roughness remains typically on the order of 5nm almost independent of the type of lithography used in production [51]. Line-edge and line-width

roughness does not scale accordingly as the technology scaling, becoming an increasingly larger fraction of the gate length. LER and LWR will result in the increases in the subthreshold current [52] and the degradation in the threshold voltage (V_T) characteristics [53]. The variation effect due to LER and RDF are statistically independent and can be modeled independently [54].

The scaling of the MOSFETs to deep submicrometer involves aggressive reduction in the gate oxide thickness. When the oxide thickness is equivalent to only a few silicon atomic layers, the atomic scale interface roughness steps between Si-SiO₂ and SiO₂-polysilicon gate will result in significant oxide thickness variation (OTV) within the gate region. Asenov et al. [55] show that intrinsic threshold voltage fluctuations induced by local oxide thickness variations become comparable to voltage fluctuations introduced by RDF for conventional MOS devices with dimensions of 30nm and below. A V_{TH} fluctuation of about 30 mV is produced due to gate oxide thickness fluctuation by interface roughness for an MOSFET with $L=W=30\text{nm}$.

Furthermore, the presence of fixed charge and fast transient charging of electron traps in the high-k layer can also cause the mobility degradation and the threshold voltage instability.

CHAPTER 3 : DESIGN FOR RELIABILITY USING ADAPTIVE GATE-SOURCE BIASING

3.1 Adaptive Gate-Source Biasing

An adaptive gate-source biasing scheme is used to produce a stable drain current robust to threshold voltage drift or mobility degradation from device stress degradations. The adaptive gate-source biasing schematic is shown in figure 3.1 [20].

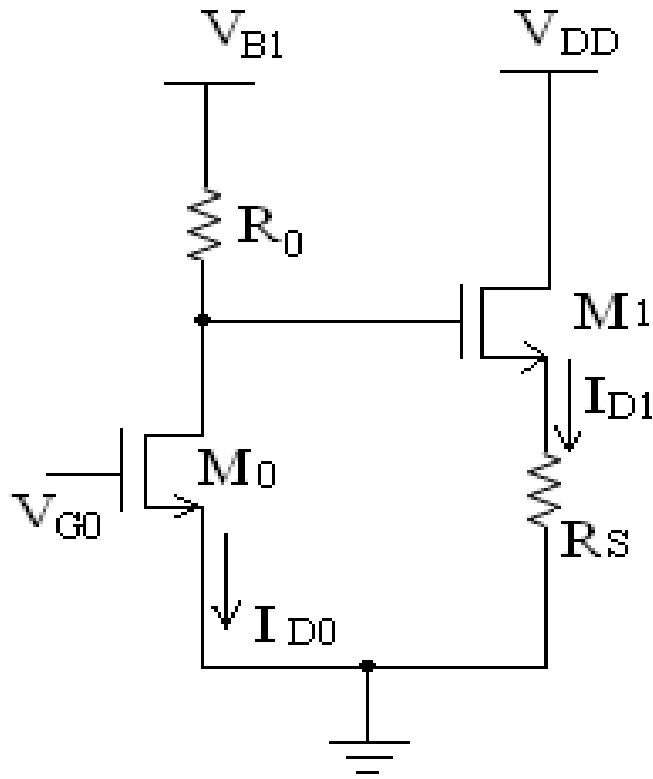


Figure 3.1 Schematic of adaptive gate-source biasing.

The gate voltage of transistor M1 is set by the biasing circuit of M0 and R0, and the source of M1 is connected with R_S . The analytical equation for drain current of the transistor M1 in the saturation region can be expressed as:

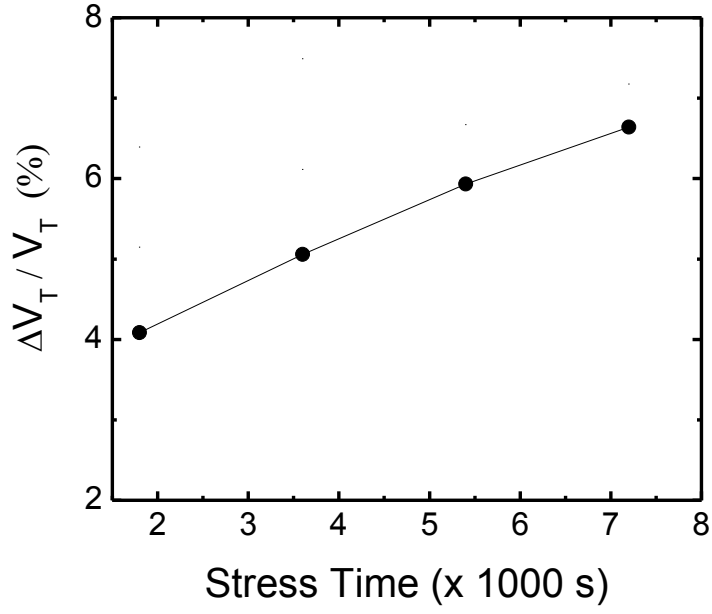
$$I_{D1} \approx \frac{\mu_n C_{ox} W}{2L} (V_{B1} - I_{D0} R_0 - I_{D1} R_S - V_{T1})^2 \quad (3.1)$$

Where W is the channel width, L is the channel length, C_{ox} is the oxide capacitance, and V_{T1} is the threshold voltage of M1.

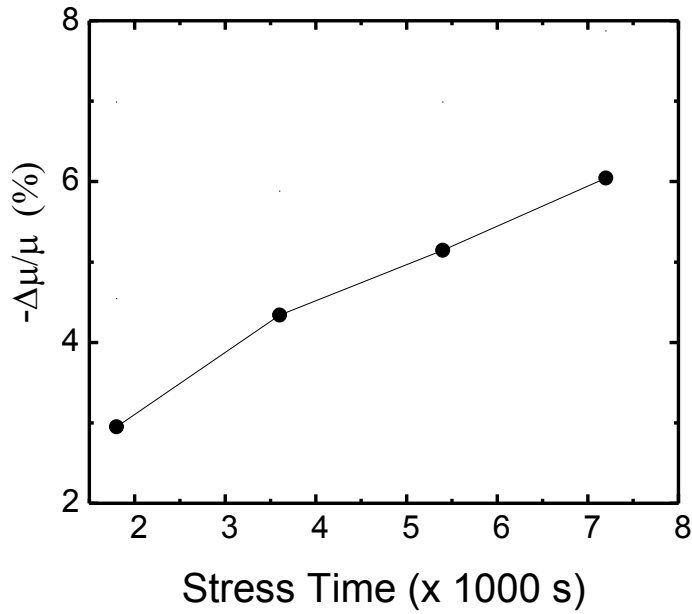
After the long term voltage stress applied to transistors M1 and M0, the threshold voltages of M1 and M0 increase simultaneously due to their identical stress conditions. The drain current of M0 decreases, thus the ohmic loss on resistor R0 reduces. The gate bias of M1 increases since $V_{g1} = V_{B1} - I_{D0} R_0$. In addition, the drain current of M1 decreases due to the increase of its threshold voltage which results in the source voltage of M1 decreases since $V_{s1} = I_{D1} \times R_S$. Therefore, the gate-source voltage of M1 increases. It could keep $V_{gs1} - V_{T1}$ stable to maintain a constant drain current of transistor M1. Similarly, the adaptive gate-source biasing scheme can also be applied to the stress induced mobility degradation. The reduction in electron mobility μ_n after stress can decrease the drain current of M0 and M1. Consequently, the gate biasing of M1 increases, the source voltage of M1 decreases, the gate-source voltage of M1 increases which in turn to maintain a relatively stable drain current I_{D1} . Therefore, using the adaptive gate-source biasing scheme can keep the drain current of M1 relatively constant regardless the threshold voltage drift and mobility reduction after device stress degradations.

Although the physical mechanisms of the hot carrier effect, the gate oxide SBD and the negative-bias temperature instability are totally different and occurrence of degradations may be

at different locations of MOS transistors under different biases, they all cause common device parametric drifts, namely, the threshold voltage shift and the mobility degradation from the circuit-design point of view. The measured normalized threshold voltage drift and mobility degradation as a function of stress time subjected to different stress conditions are shown in Fig. 3.2. The devices under test are $0.16 \times 20 \mu\text{m}^2$ nMOSFETs. The gate oxide thickness of the transistor is 2.4 nm. The gate-source and drain-source voltages of the transistors were kept the same at a high voltage ($V_{\text{DS}} = V_{\text{GS}} = 2.8 \text{ V}$) at the room temperature, where the transistors were biased under the hot electron and the gate oxide stress. I-V measurement was taken periodically for parameter extraction. The threshold voltage and the mobility were extracted using BSIMPro at various time points. The degradation of the device is plotted in the form of the normalized change to the original threshold voltage and mobility versus stress time as shown in Fig. 3.2 (a) and (b). From the experimental data in Fig. 3.2, we can conclude that the threshold voltage increases and the mobility decreases as a function of stress time.



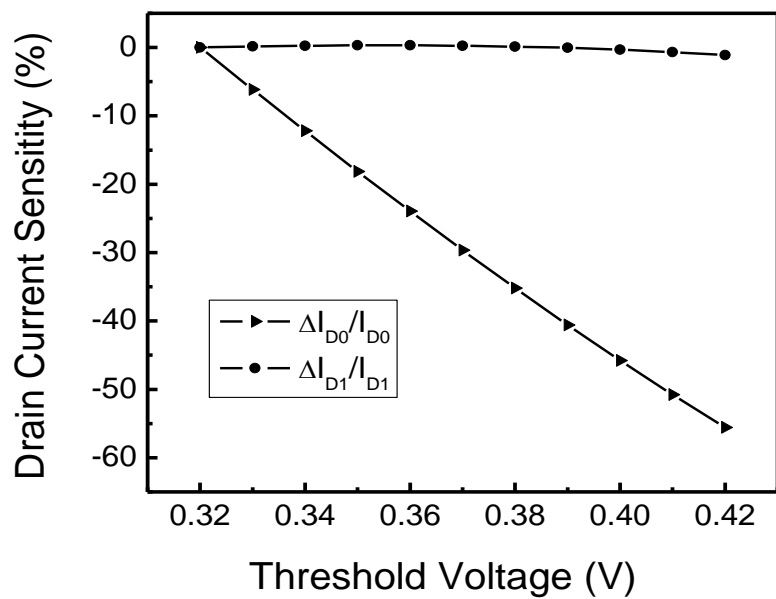
(a)



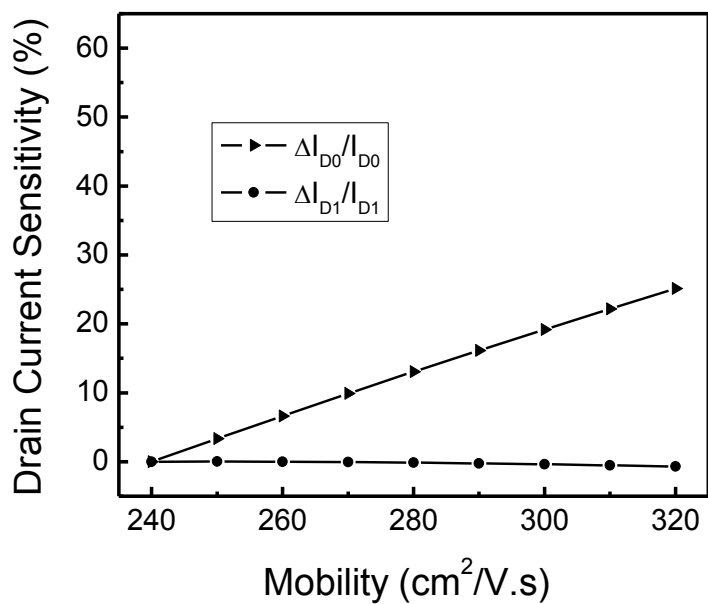
(b)

Figure 3.2 Measured (a) threshold voltage and (b) mobility variations versus stress time. Stress conditions: $V_{GS} = 2.8$ V and $V_{DS} = 2.8$ V at room temperature. The transistor oxide thickness (EOT) is 2.4 nm.

The validation of the adaptive gate-source biasing scheme is demonstrated in Fig. 3.3. In this simulation, M0 and M1 are set to have identical bias (stress) conditions ($V_{GS0} = V_{GS1}$ and $V_{DS0} = V_{DS1}$) by choosing appropriate bias conditions. Here, the bias of the circuit is set as following: $V_{G0} = 0.7$ V, $V_{B1} = 1.05$ V, $V_{DD} = 1.5$ V, $R_0 = 3.2$ Ω and $R_S = 10$ Ω . Both transistors have a channel length of 0.18 μm and a channel width of 900 μm . The drain current plots of M0 and M1 are generated by sweeping the threshold voltage and the mobility independently versus the threshold voltage and the mobility drifts normalized to their corresponding fresh values as shown in Fig. 3.2. Fig. 3.3 (a) shows the normalized drain current of transistor M1 and M0 as a function of threshold voltage and Fig. 3.3 (b) shows the normalized drain current of transistor M1 and M0 versus mobility degradation. The drain current I_{D0} of the transistor M0 drastically changes when the threshold voltage increases and the mobility decreases. However, by choosing the appropriate resistance values of R_0 and R_S , the drain current I_{D1} of the transistor M1 can be insensitive to the threshold voltage and the mobility variations due to adaptive gate-source biasing for M1.



(a)



(b)

Figure 3.3 Normalized drain current versus (a) threshold voltage (b) mobility

3.2 RF Power Amplifiers Fundamentals

3.2.1 Power Amplifier Class

Power amplifiers can be categorized into different types (A, AB, B, C, D, E, F) distinguished primarily by bias conditions and conduction angle. For the four classic classes A, AB, B and C, the input signal overdrive is relatively small and the device is operated more as a current source. Class A, AB, B, and C may be studied with a single model as in Fig. 3.4 [56].

In this general model, the resistor R_L represents the load. The RF choke feeds DC power to the drain. The RF choke is assumed large enough so that the current through it is substantially constant. The matching network formed with LC tank is used to optimize gain. The drain voltage of the output transistor swings between ground and $2V_{DD}$ depending on the input power level.

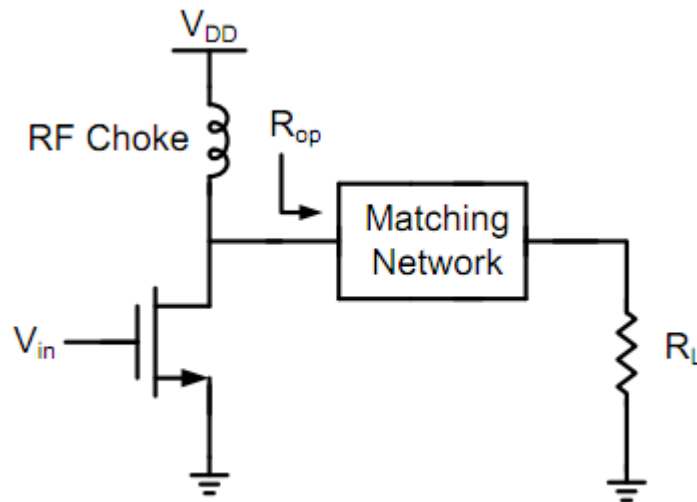


Figure 3.4 General power amplifier model

The current and voltage waveforms of class A, AB, B and C power amplifiers are shown in Fig. 3.5. Class A power amplifier is operated in full input and output range which provides good linearity at the cost of low efficiency. For class AB, B and C, the gate bias voltage is decreased

to reduce the conduction angle for higher efficiency as illustrated in Fig. 3.5. The maximum efficiency for class A is 50%. With a smaller conduction angle, the power efficiency of class AB can reach up to 78.5%. For class C, as the conduction angle shrinks to zero, the efficiency can reach 100%. θ

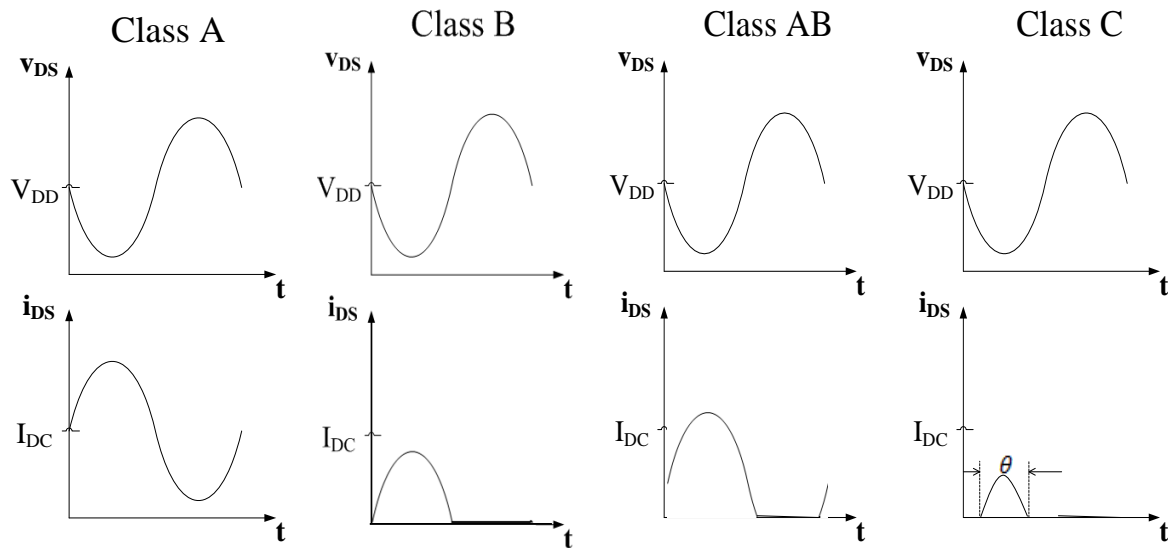


Figure 3.5 Current and voltage waveforms of class A, AB, B and C power amplifiers.

For class D, E and F power amplifiers, the transistor is used as a switch. The current and voltage waveforms for class D, E and F power amplifiers are shown in Fig. 3.6. Since there is either zero voltage across it or zero current across it, the transistor dissipates no power and the theoretical efficiency is 100%.

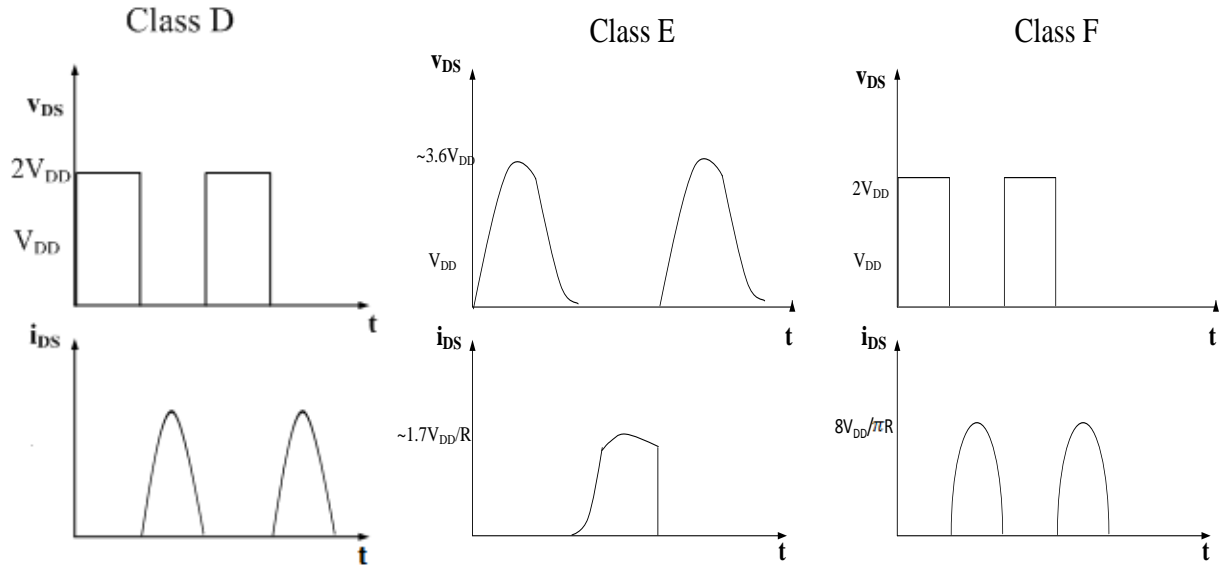


Figure 3.6 Current and voltage waveforms of class D, E and F power amplifiers.

3.2.2 Power Amplifier Performance Parameters

3.2.2.1 1dB Compression Point

1dB compression point is defined as the power level at which the output power has reduced by 1dB from the ideal characteristic. 1 dB compression point can be stated in terms of either input power or output power. The definition of the 1 dB compression point for a nonlinear power amplifier is shown in Fig. 3.7. Gain compression occurs when the input power of an amplifier is increased to a level that reduces the gain of the amplifier and causes a nonlinear increase in output power. 1 dB compression point is used to characterize the nonlinearity of a power amplifier [57].

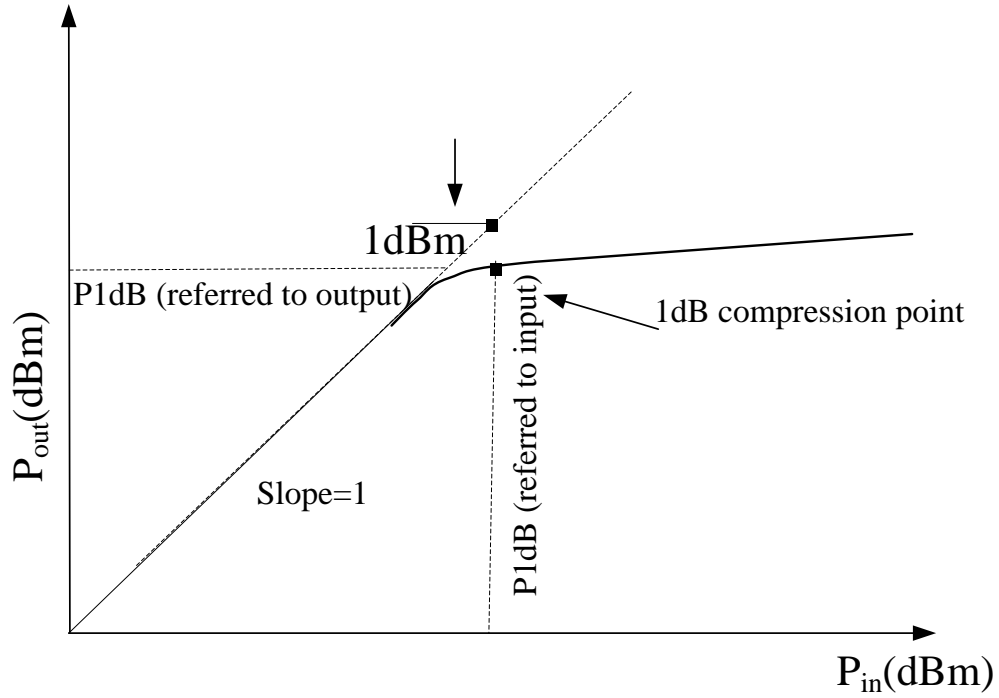


Figure 3.7 Definition of the 1dB compression point for a nonlinear amplifier

3.2.2.2 Third Order Intercept Point

The third order intercept point is to measure the nonlinearity of a power amplifier using a two tone input signal. When the power amplifier has two tone input signal as [57]:

$$v_i = V_0(\cos\omega_1 t + \cos\omega_2 t) \quad (3.2)$$

The output of the power amplifier is

$$v_o = a_0 + a_1 V_0(\cos\omega_1 t + \cos\omega_2 t) + a_2 V_0^2(\cos\omega_1 t + \cos\omega_2 t)^2 + a_3 V_0^3(\cos\omega_1 t + \cos\omega_2 t)^3 + \dots \quad (3.3)$$

Third order intermodulation products are obtained by using trigonometric manipulation.

The third order intermodulation products $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ located near the original

signals at ω_1 and ω_2 , and so cannot be easily filtered from the pass band of the amplifier. The resulting in-band intermodulation products will cause distortion of the output signal.

The third order intercept point is the intersection point where the extension of the idealized response of the first order term and the third order term intersects. The input-referred third-order intercept point (IIP3) is specified as an input power. The third order intercept diagram for a nonlinear power amplifier is shown as in Fig. 3.8 [57].

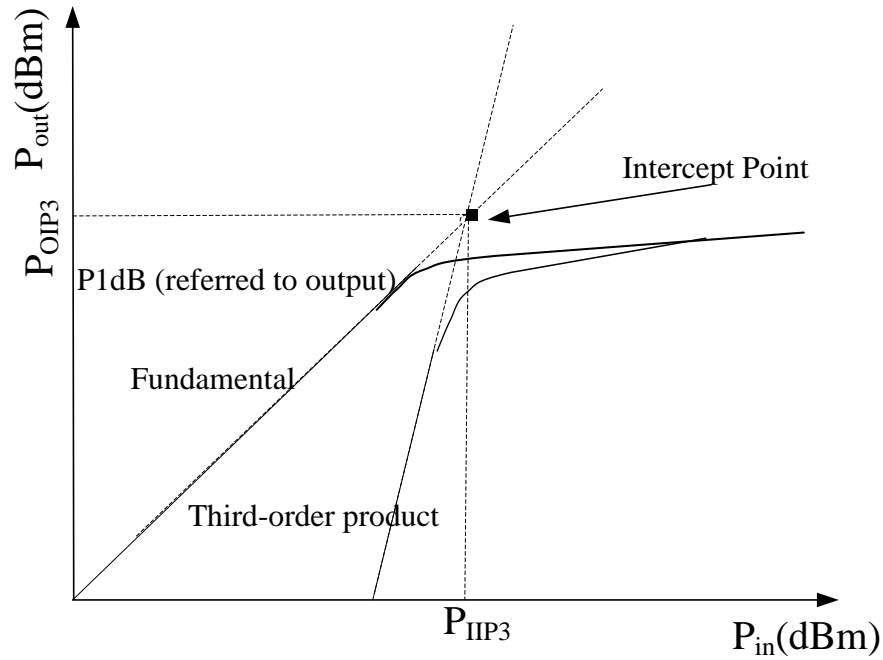


Figure 3.8 Third-order intercept point for a power amplifier

3.2.2.3 Drain Efficiency and Power Added Efficiency

The drain efficiency of a power amplifier is defined as

$$\eta_{drain} = \frac{P_o}{P_{DC}} \quad (3.4)$$

Where P_o is the output power and P_{DC} is the dc consumption of a power amplifier.

Here, the drain efficiency of class-A and class-AB power amplifiers can be written as [56]

$$\eta = \frac{V_m}{V_{DD}} \frac{\theta - \sin \theta}{4 \left(\sin \frac{\theta}{2} - \frac{\theta}{2} \cos \frac{\theta}{2} \right)} \quad (3.5)$$

Where V_{DD} is the supply voltage, V_m is the maximum output voltage and θ is the conduction angle. When the conductance angle decreases, the maximum drain efficiency increases if the maximum output voltage is the same.

For the power amplifier, a more realistic measure of efficiency is the power-added efficiency defined as:

$$\eta_{add} = \frac{P_o - P_i}{P_{DC}} \quad (3.6)$$

Where P_i is the input power to the power amplifier, P_o is the RF output power and P_{DC} is the transistor dc power dissipation. The maximum power added efficiency generally occurs around the 1 dB gain compression point for a matched power amplifier.

3.3 RF Power Amplifier with Adaptive Gate-Source Biasing

Here, the device degradations in relation to RF circuit performance degradations and design for reliability by using adaptive gate-source biasing to improve the RF circuit reliability are studied. A RF power amplifier designed at 900 MHz with adaptive gate-source biasing is shown in Fig. 3.9. The channel length of the n-channel transistor is 0.18 μm , the channel width is 900 μm , and the threshold voltage is 0.34 V. The RF tank has $C1 = 30$ pF and $L1 = 1$ nH to short high-order harmonics. The supply voltage is $V_{DD} = 1.5$ V and the gate bias $V_{bias} = 700$ mV. The

device is biased to a quiescent point so that the power amplifier is operated in the class-AB mode at input power of 0 dBm.

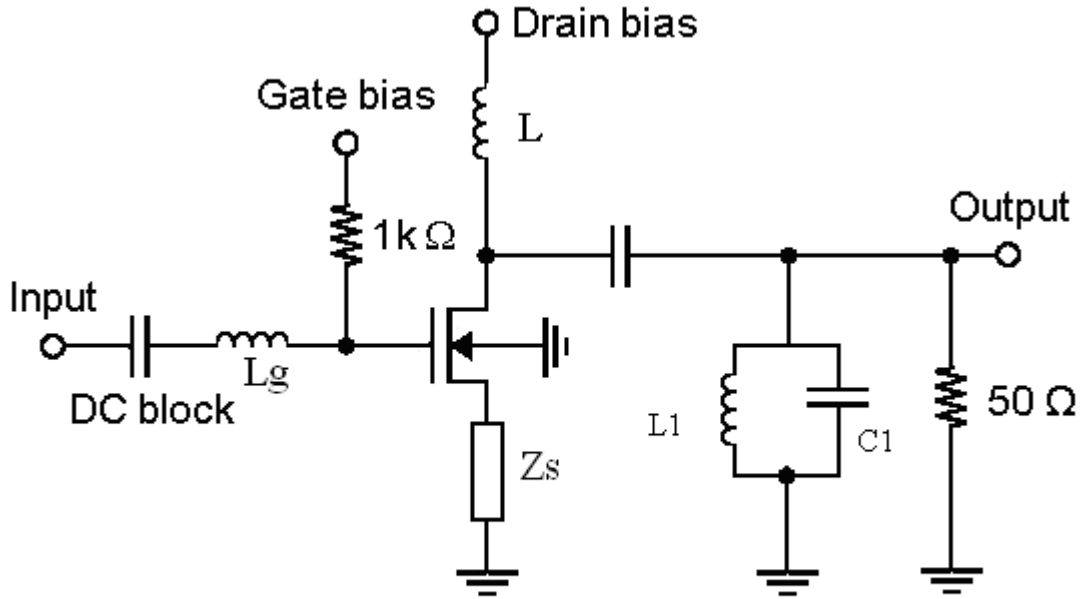
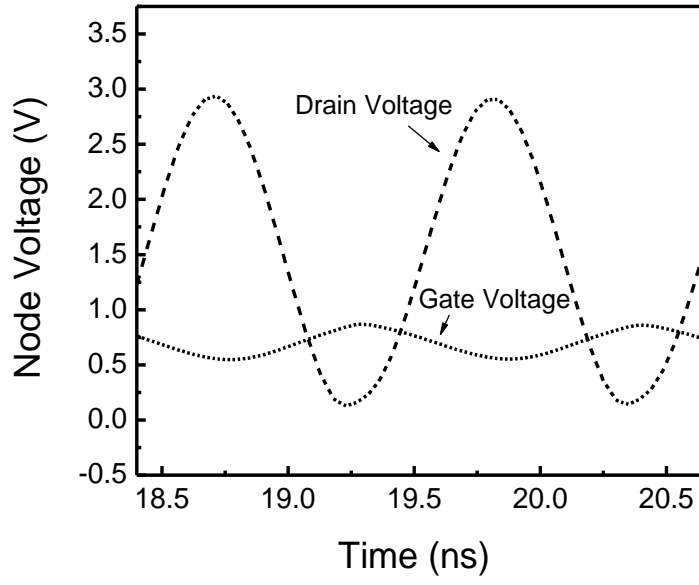
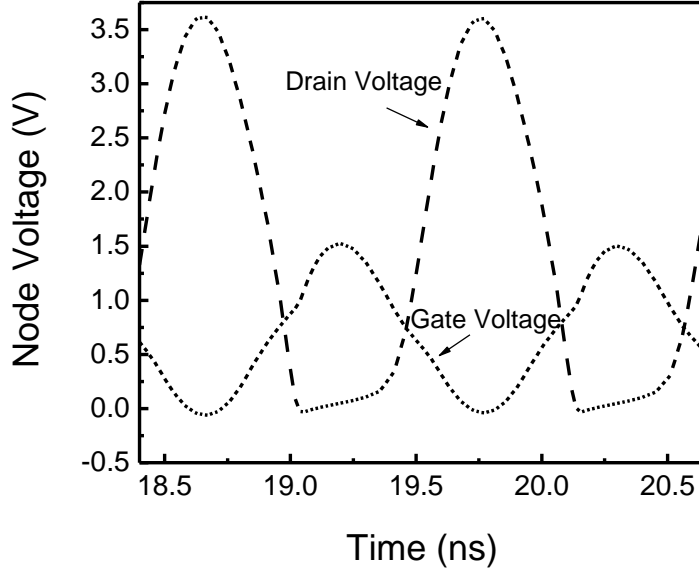


Figure 3.9 A class-AB RF power amplifier with source impedance.

The gate-source and drain-source voltages versus time are obtained using Cadence SpectreRF simulation at the input RF power $P_i = -10$ dBm and 0 dBm, as displayed in Fig. 3 10 (a) and (b), respectively. At the input power of -10 dBm, the power amplifier is operated at the class A mode with a fundamental frequency of 900 MHz. The n-channel transistor is subjected to hot electron stress due to continued on period at high V_{DS} . At the input power of 0 dBm, the power amplifier is operated at the class AB mode. The channel transistor is mainly subjected to the Fowler–Nordheim stress due to a high drain-to-gate voltage.



(a)



(b)

Figure 3.10 Simulated drain-source voltage and gate-source voltage versus time (a) $P_i = -10$ dBm,

(b) $P_i = 0$ dBm

The power amplifier without any source bias component, with source resistance ($R_S = 30 \Omega$), with source inductance ($L_S = 2 \text{ nH}$), and with both the source resistance and inductance in series ($R_S = 5 \Omega$ and $L_S = 1 \text{ nH}$) are examined. The time-dependent drain current and gate-source voltage before and after stress with and without source biasing with input power of -10 dBm are shown in Fig. 3.11 and Fig. 3.12, respectively.

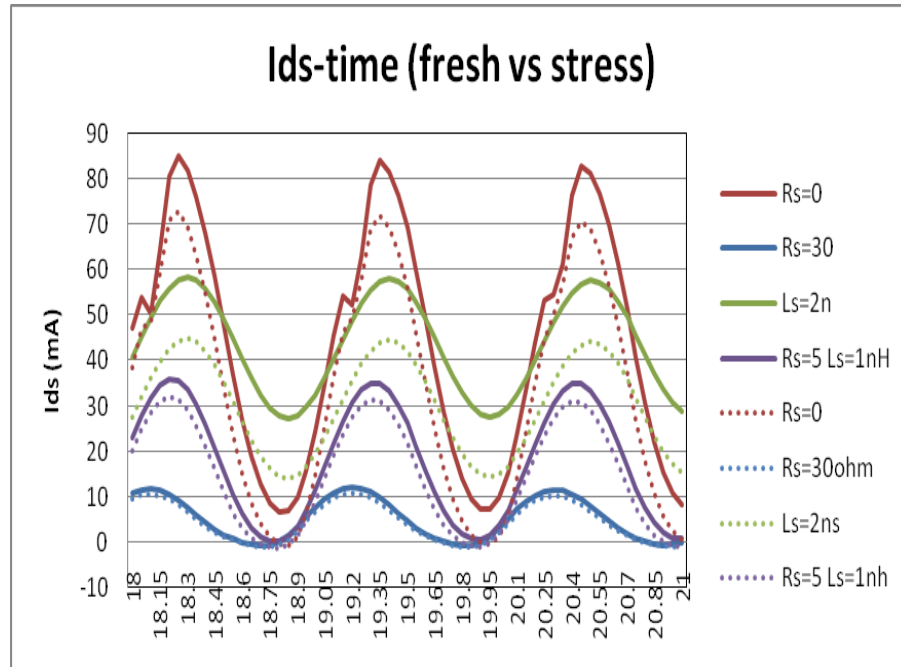


Figure 3.11 Waveforms of I_{ds} versus time at fresh and stress condition with and without source biasing impedance

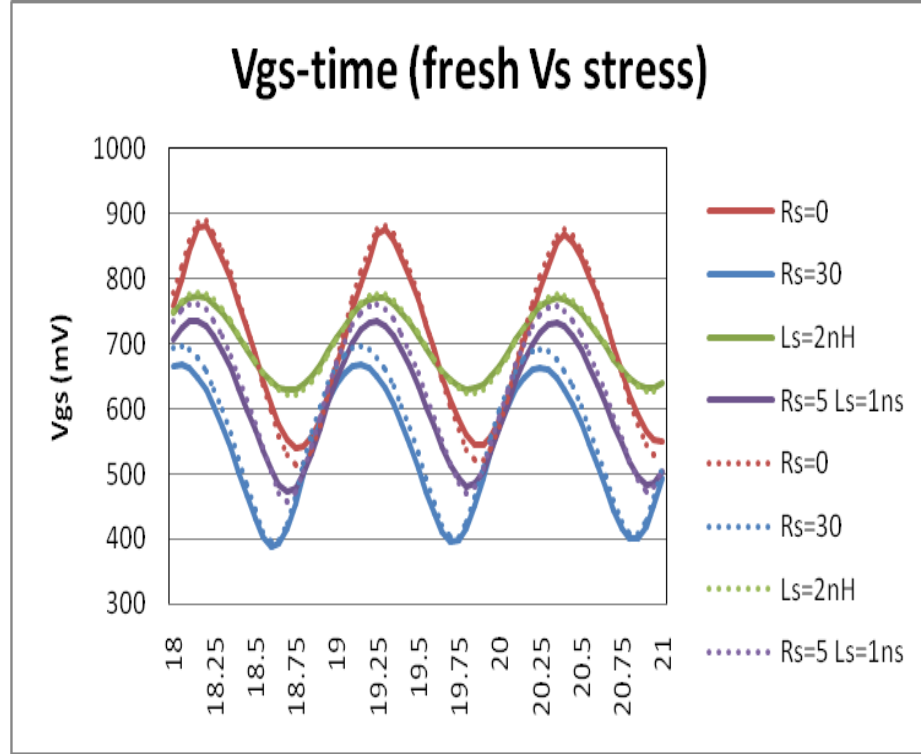
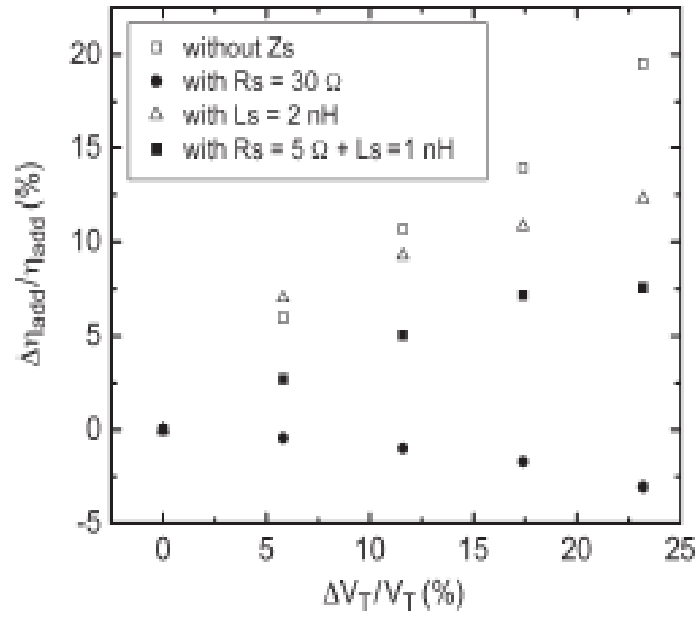
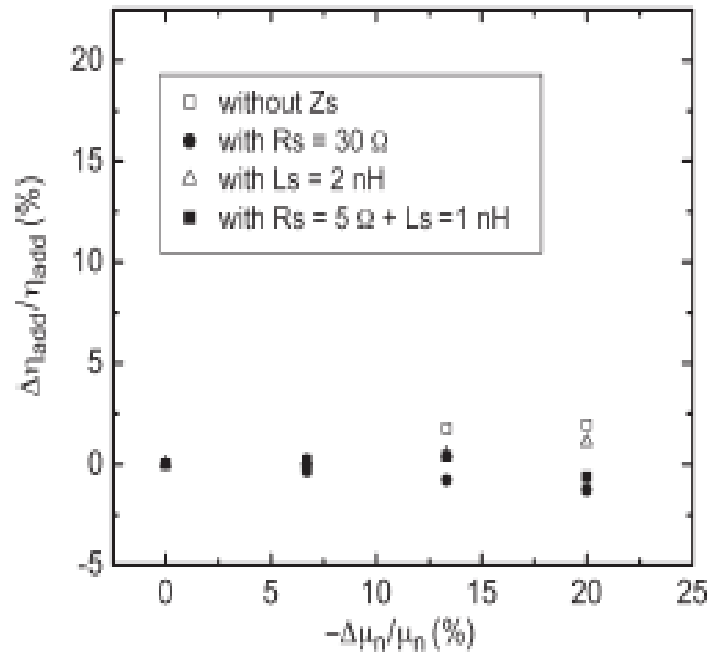


Figure 3.12 Waveforms of V_{GS} versus time at fresh and stress condition with and without source biasing impedance

The normalized power-added efficiency η_{add} as a function of the threshold voltage variation $\Delta V_T/V_T$ and the electron mobility reduction $-\Delta\mu_n/\mu_n$ using the Cadence SpectreRF simulation are shown in Fig. 3.13. In the Cadence simulation, V_{TH0} and U_0 are independently swept to generate the sensitivity data. This gives us an insight into how the threshold voltage and the mobility drift individually change the RF performance. In Fig. 3.13, the empty squares represent the original power amplifier without any source component Z_S , the solid circles represent the PA redesigned with the source resistance ($R_S = 30 \Omega$), the empty triangles represent the PA with the source inductance ($L_S = 2 \text{ nH}$), and the solid squares represent the PA with both the source resistance and inductance in series ($R_S = 5 \Omega$ and $L_S = 1 \text{ nH}$).



(a)



(b)

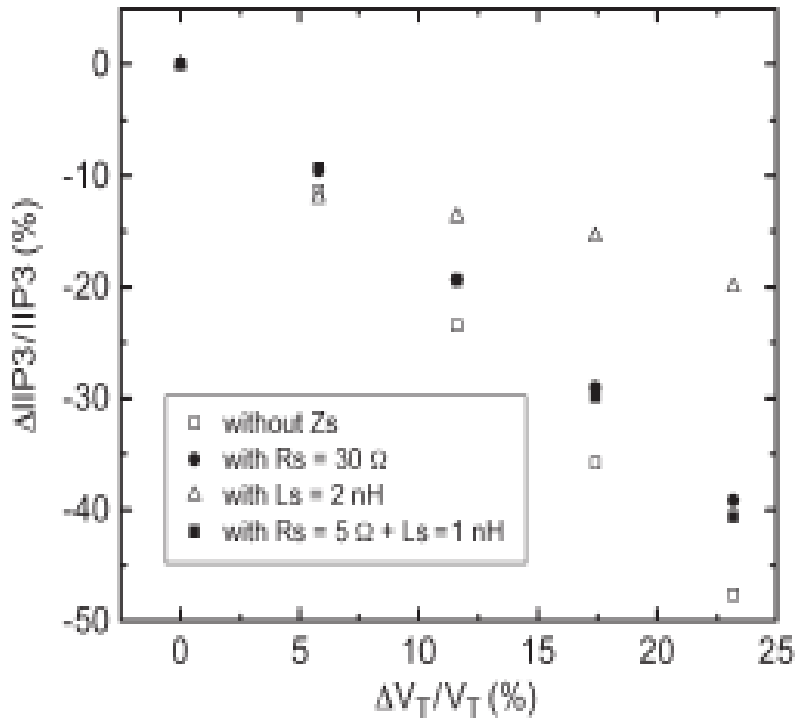
Figure 3.13 Normalized power-added efficiency versus normalized (a) threshold voltage shift (b) mobility variation. The power-added efficiency was extracted at $P_i = -0.5\ \text{dBm}$

As seen in Fig. 3.13, the source resistance used in the power amplifier significantly improves the sensitivity of the normalized power-added efficiency by providing adaptive gate-source biasing. The value of source resistance needs to be selected appropriately considering the performance and the reliability. For example, a large source resistor could result in power-added efficiency degradation, whereas a small source resistor may not provide enough feedback effect. A large source inductor will significantly increase the circuit size. The use of R_S and L_S in series is a compromise design to optimize the performance and the reliability together. The optimization can be done by a simulation approach or an experimental tuning.

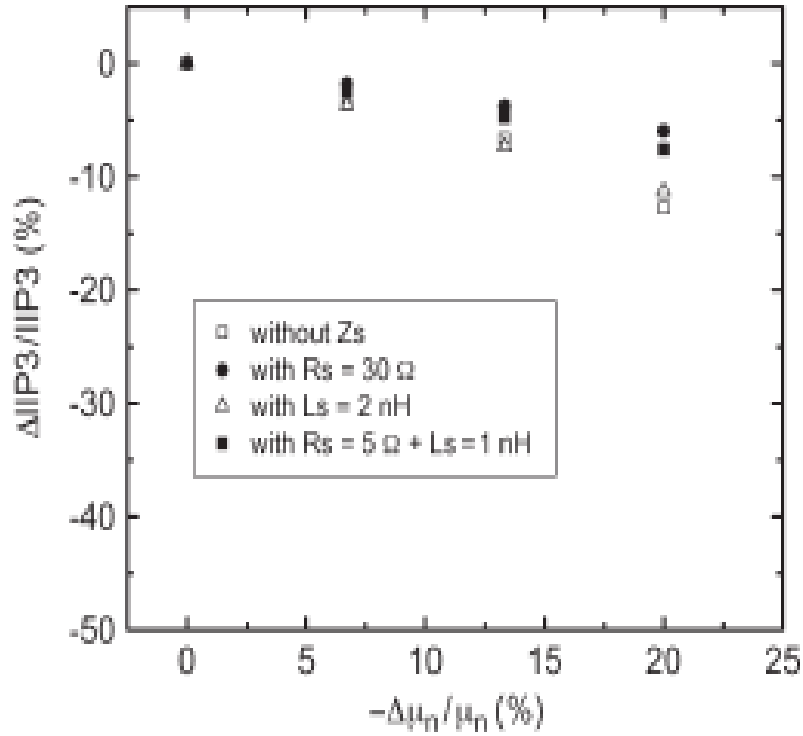
In Fig. 3.13 (a), the increase in $\Delta\eta_{add}/\eta_{add}$ for the PA without Z_S or with L_S is due to the conduction angle θ reduction when the threshold voltage increases after stress. In Fig. 3.13 (b), the mobility degradation would increase the normalized power-added efficiency of the PA without source compensation due to the decrease of the DC power dissipation of the MOS transistor. Comparing Fig. 3.13 (a) with Fig. 3.13 (b), the normalized power-added efficiency is more sensitive to the threshold voltage shift than the mobility reduction because the bias point V_{GS} is close to V_T (the closer the V_{GS} to V_T , the higher the impact of the threshold voltage shift). The most effective way to improve the power efficiency sensitivity is the use of source resistor as shown in Fig. 3.13 (a).

The simulated input third-order intercept point variation $\Delta IIP3/IIP3$ as a function of the threshold voltage and the mobility variations normalized to their fresh values are shown in Fig. 3.14 (a) and (b), respectively. The input third-order intercept point $IIP3$ is the cross-point between the fundamental RF output power and the third-order harmonic power referred to the input power. Again, in Fig. 3.14, the empty squares represent the original power amplifier

without any source compensation, the solid circles represent the PA using the source resistance, the empty triangles represent the PA redesigned with the source inductance, and the solid squares represent the PA using R_S and L_S in series. As the normalized power-added efficiency, the normalized input third-order intercept is also more sensitive to the threshold voltage shift than the mobility variation by comparing Fig. 3.14 (a) and (b). As shown in Fig. 3.14 (a), the use of the source inductance is the most effective way to suppress the $IIP3$ variation subject to threshold voltage shift.



(a)



(b)

Figure 3.14 Normalized $IIP3$ variation versus normalized (a) threshold voltage shift and (b) mobility degradation.

3.4 Conclusion

RF circuit design for reliability is studied in this chapter. Although the hot electron damage and gate oxide breakdown have totally different reliability physics and occur at different locations in MOSFETs, they all result in mobility and threshold voltage degradation from the circuit degradation's point of view. The adaptive gate-source biasing scheme is developed to improve the circuit reliability against device degradation. The adaptive gate-source biasing scheme can get a stable DC drain current independent of threshold voltage and mobility

variations. A class-AB PA power amplifier is used for validate the methodology. The use of a source inductance is more robust for the third-order intercept point or linearity, while the use of a source resistance is more effective in achieving a stable power-added efficiency against device parametric variations.

CHAPTER 4 : CMOS RF POWER AMPLIFIER FOR VARIABILITY AND RELIABILITY IMPROVEMENT WITH GATE BIASING

4.1 Circuit Design

A RF power amplifier designed at 24 GHz with adaptive gate biasing is shown in Fig. 4.1. All the n-channel transistors are modeled using PTM 65 nm technology [58]. The channel width of the main transistor M1 is 50 μm , and the width of the bias transistor M2 is 20 μm . The supply voltage V_{dd} is 1 V and the gate voltage of M2 is set to 0.6 V. The gate voltage of M1 is determined by the drain voltage of M2 which will change when both the M1 and M2 after electric stress instead of fixed bias voltage. The bias resistors R1 and R2 are given in Fig 4.1, $R_1 = 200 \Omega$, $R_2 = 45 \Omega$ to provide proper gate bias voltage for transistor M1.

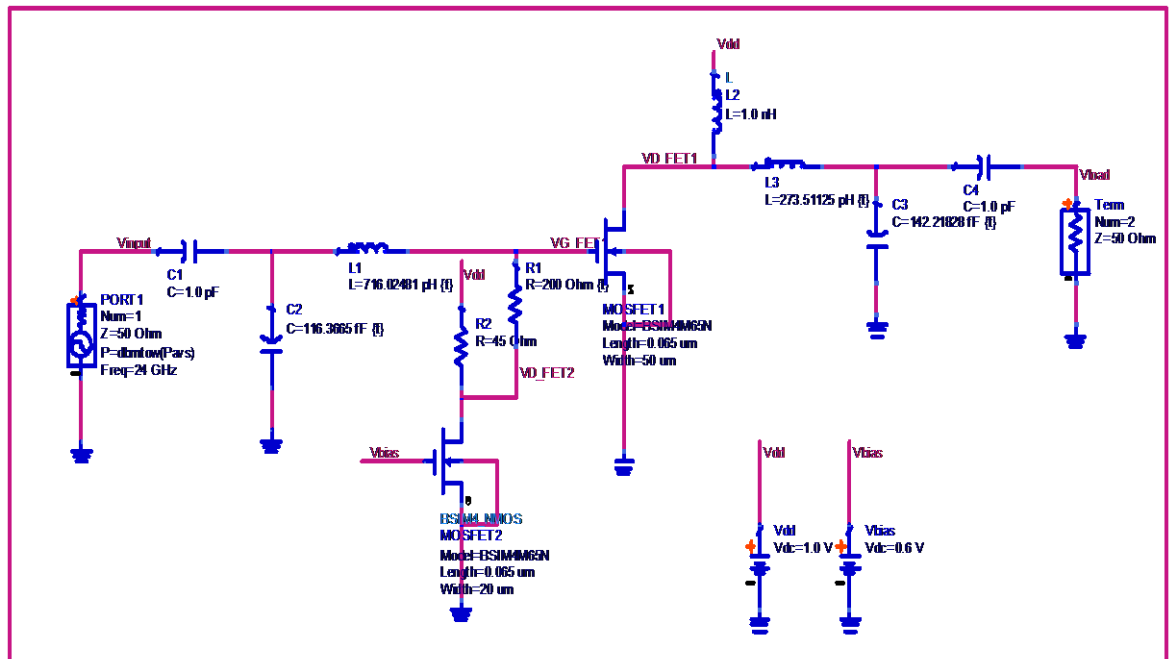


Figure 4.1 A RF power amplifier with gate biasing

Fig. 4.2 (a)-(d) show the output power (P_{out}), power gain and power-added efficiency (PAE) sensitivity subject to threshold voltage variation caused by process variation or stress degradation. The results were obtained from ADS simulations by changing threshold voltage from 0.42 V to 0.5 V with a 0.02 V changing step. The output power variation versus threshold variation for power amplifier with gate biasing and without gate biasing was shown in Fig. 4.2 (a). As the input power changing from – 20 dBm to 0 dBm , the output power variation for PA with gate bias is less than the PA without gate biasing for the same threshold voltage variation. Fig. 4.2 (b) shows the power gain sensitivity for the threshold voltage variation, the similar conclusion can be got that the power gain of PA with gate biasing is less sensitive for threshold voltage variation than that of the PA without gate biasing. The power-added efficiency sensitivity for PA without gate biasing and PA with gate biasing are shown in Fig. 4.2 (c) and (d), respectively. The PAE variation has been improved a big degree with gate biasing method compared to that without gate biasing. Fig. 4.3 (a)-(d) are the P_{out} , power gain and PAE sensitivity subject to mobility degradation. Similar to the case for the threshold voltage variation, the power amplifier with gate biasing improved the sensitivity for the circuit performance versus mobility variation. Comparing Fig. 4.2 with Fig. 4.3, the output power, power gain and power-added efficiency are more sensitive to the variation of the threshold voltage than the variation of the mobility.

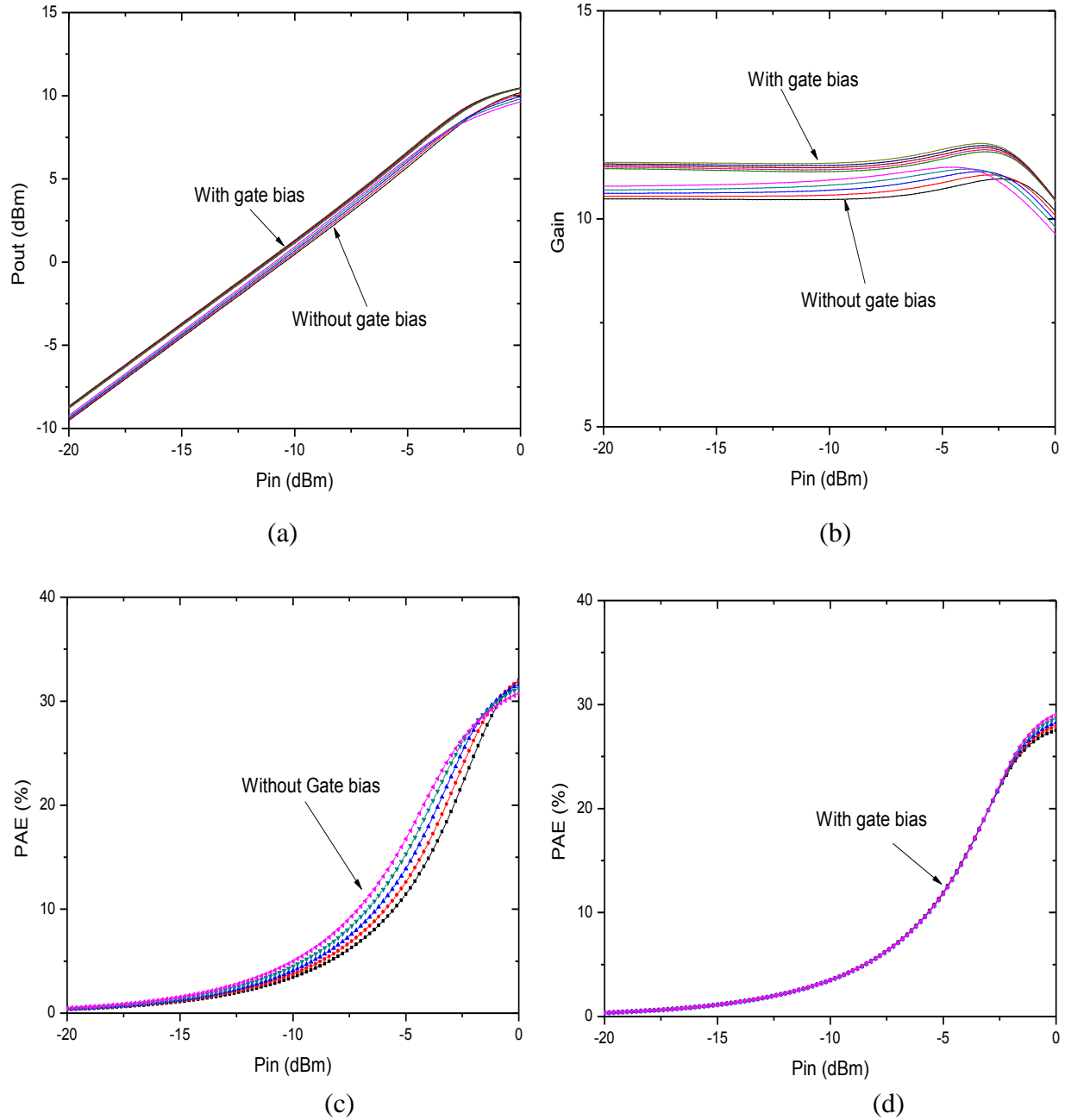


Figure 4.2 (a) P_{out} variation for PA with and without gate biasing (b) power gain variation for PA with and without gate biasing (c) PAE variation for PA without gate biasing (d) PAE variation for PA with gate biasing versus transistor threshold voltage variation (V_{th} changes from 0.42 V~0.50 V by 0.02 V step)

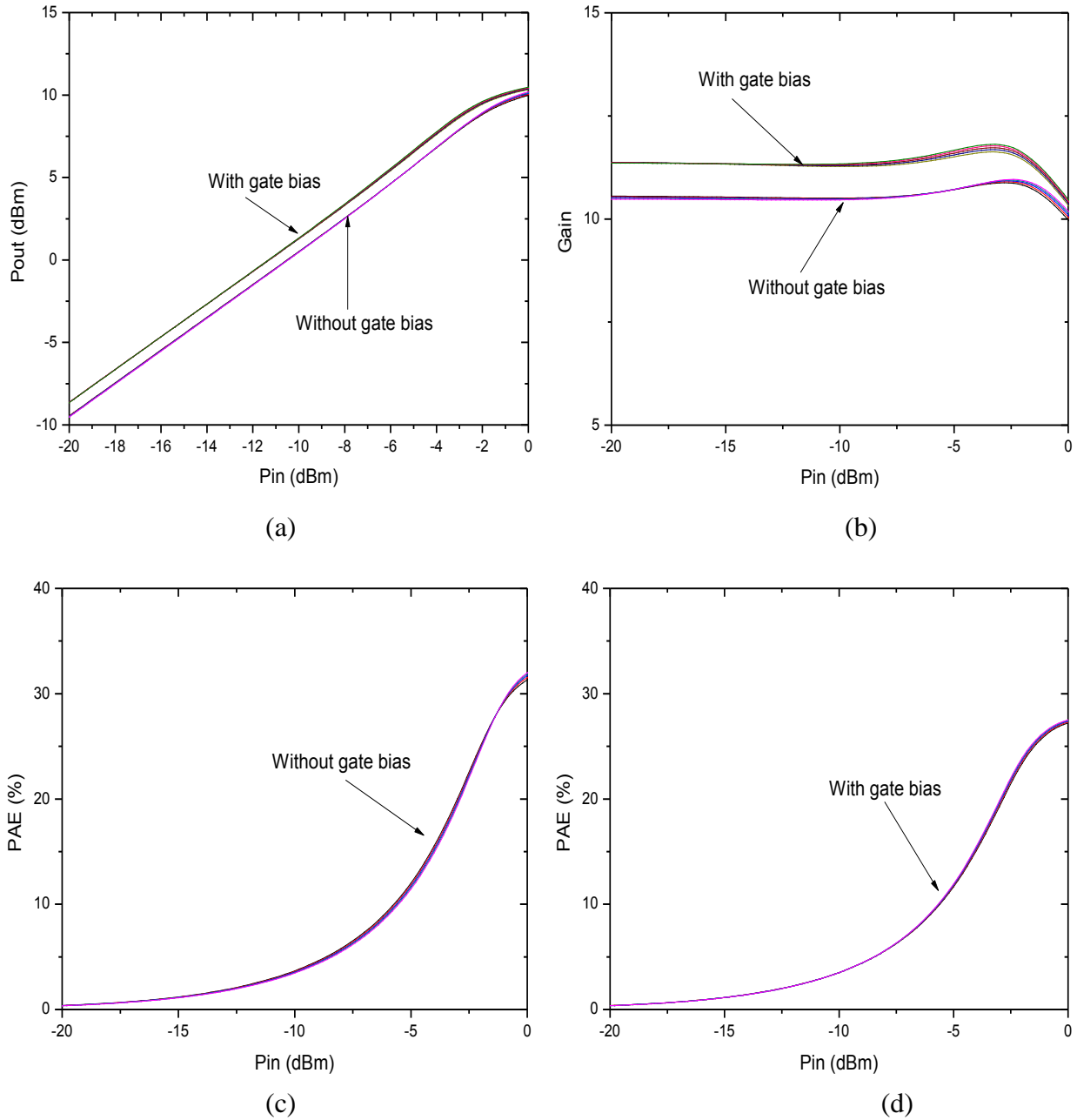
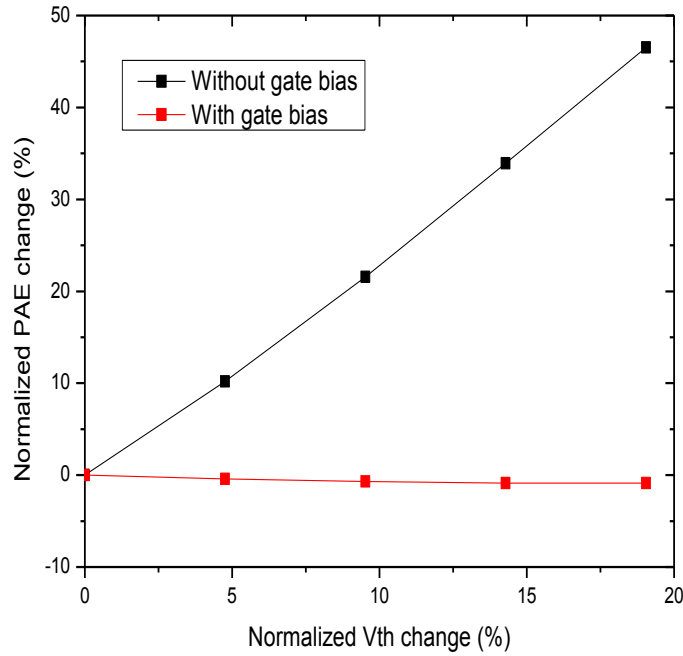
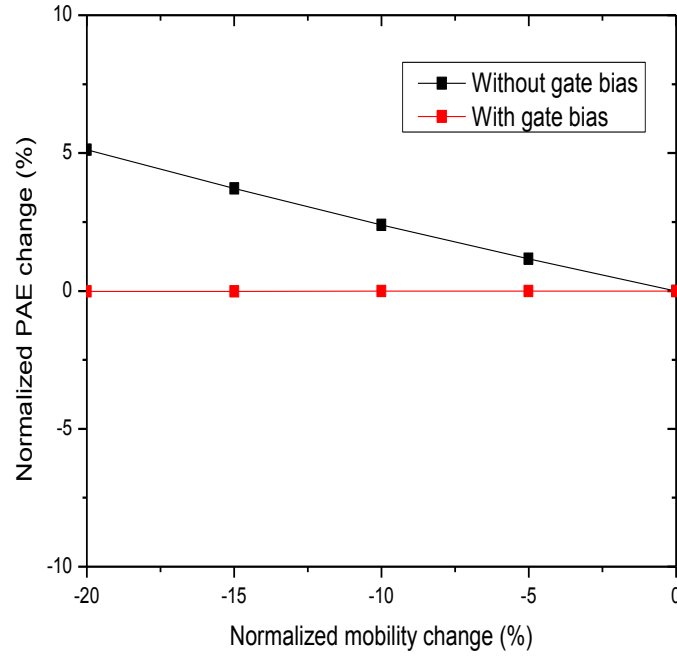


Figure 4.3 (a) P_{out} variation for PA with and without gate biasing (b) power gain variation for PA with and without gate biasing (c) PAE variation for PA without gate biasing (d) PAE variation for PA with gate biasing versus mobility variation (μ_n changes from 0.0491~0.03928 $m^2/(V.s)$ with 5 steps)

Fig. 4.4 (a) and (b) display the simulated normalized power-added efficiency variation $\Delta PAE/PAE$ for power amplifier with and without gate bias in the function of the threshold voltage and the mobility variations normalized to their fresh values, respectively. The black lines with squares represent the original power amplifier without gate bias and the red lines with squares represent the power amplifier redesigned with gate bias. The PAE is obtained at input power of -5 dBm. As shown in Fig. 4.4 (a), for the threshold voltage changed 20%, the PAE changed 46% for the PA without gate bias while there is only about -1% change for the PA with gate bias. For the 20% change of mobility, the PAE change for the PA without gate bias is 5.1% while the PAE change for PA with gate bias is 0.23% shown in Fig. 4.4 (b).



(a)



(b)

Figure 4.4 (a) Normalized PAE change versus normalized threshold voltage change (b) normalized PAE change versus normalized mobility change for PA with and without gate biasing

Fig. 4.5 (a) and (b) show Monte Carlo simulation of the power-added efficiency sensitivity subject to process variations. The Monte Carlo simulation is set at the condition of 10% threshold voltage variation, 10% mobility variation and 10% gate oxide variation. Comparing Fig. 4.5 (a) and (b), it is apparent that the gate biasing reduces the process variations effect significantly.

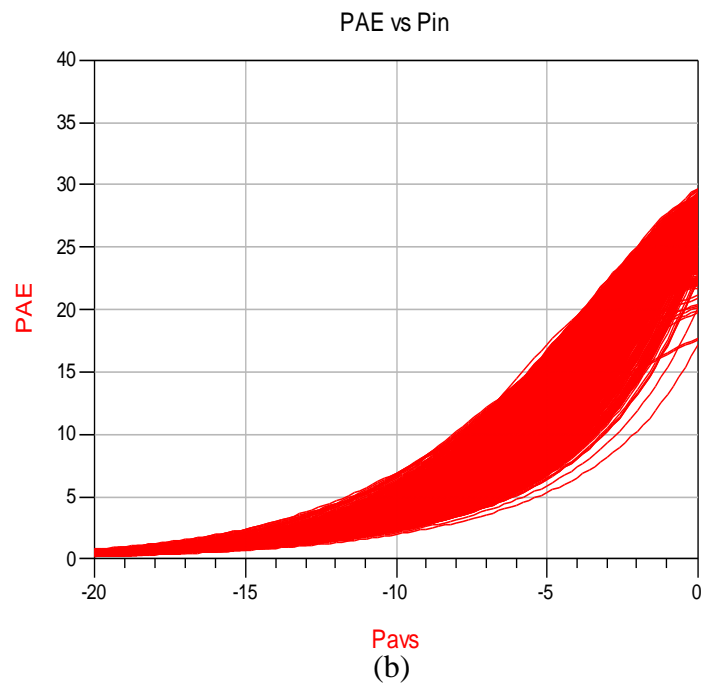
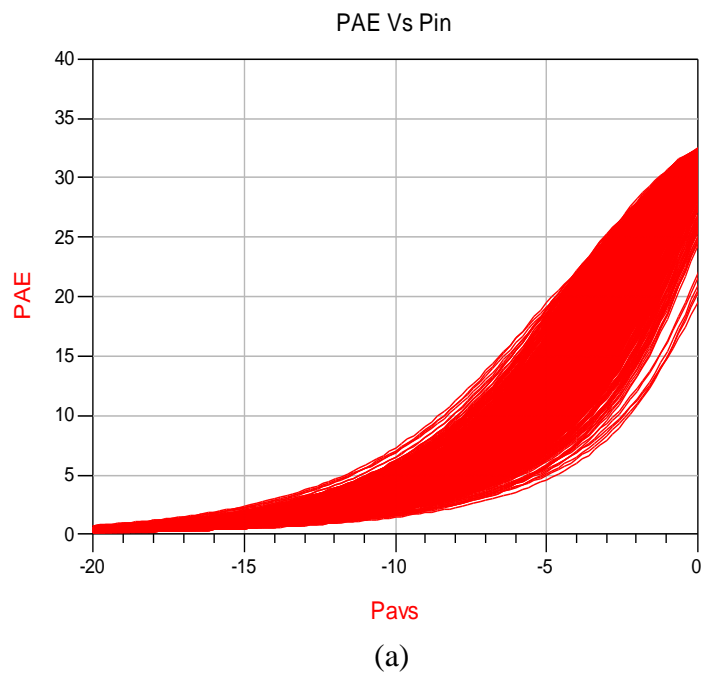


Figure 4.5 Monte Carlo simulation results for PAE variation (a) for PA without gate biasing (b)
for PA with gate biasing

4.3 Conclusion

The adaptive gate biasing technique is proposed for CMOS RF power amplifier against device reliability degradations and process variations. The power amplifier performances with adaptive gate biasing are compared with those of the power amplifier without adaptive gate biasing technique. The adaptive gate biasing reduces PAE and output power sensitivity against device aging such as mobility and threshold voltage degradation. The adaptive gate biasing also makes the power amplifier more resilient to process variations as demonstrated by Monte Carlo simulation.

CHAPTER 5 : THE PRINCIPLE OF OSCILLATOR AND INJECTION LOCK

5.1 Oscillator Fundamentals

5.1.1 Background

Oscillator is one of the most critical fundamental units in many electronic systems. It's widely used in many applications ranging from clock generation in microprocessors to frequency synthesis in cellular phones. An oscillator produces a periodically time-varying signal, usually in the form of voltage when supplied with only DC power. Any oscillator can be viewed as a two-port negative feedback back system or as a one port negative resistance system.

The two main categories of oscillators used in common wireless communication systems are ring oscillators and LC-tank oscillators. A ring oscillator is constructed by connecting an odd number series of inverters into a loop providing a 180 degree phase shift at all frequencies. The oscillation frequency of a ring oscillator is determined by the delay time of the inverters. On the other hand, a LC-tank oscillator is constructed by placing an inductor in parallel with or in series with a capacitor to form a LC resonator. The net phase shift is 0 degree at the resonance frequency of the LC tank. And the oscillation frequency of a LC tank can be tuned by using the variable capacitors (or varactors). In terms of integrability, ring oscillators are desirable due to the advantage of being fully compatible with standard digital CMOS technology and small on-chip area consumption. However, ring oscillators are usually not a good choice for high frequency application due to the huge amount of phase noise introduced as a result of positive feedback. *LC* oscillators usually provide better phase noise performance in comparison with the ring oscillators at radio

frequencies due to the higher quality factor (Q) of the LC-tank. But they are limited by the on-chip inductors and high performance capacitors which are not compatible with the standard CMOS process and consume larger area. Normally, the ring oscillator is analyzed as a two port feedback system while the LC tank is analyzed as a one port negative resistance system for convenience.

5.1.2 Two Port Feedback Model of Oscillators

The oscillator can be viewed as a linear feedback system as shown in Fig. 5.1. The closed-loop transfer function of the feedback system is given by [59]

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1+A(s)B(s)} \quad (5.1)$$

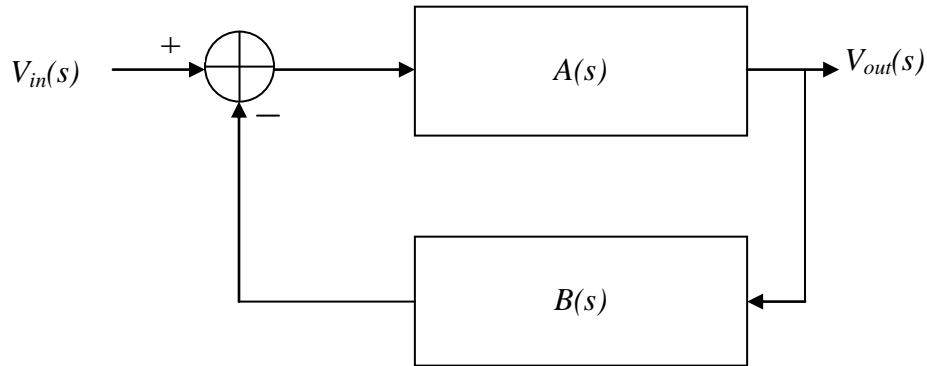


Figure 5.1 The linear model of an oscillator as a feedback system

In the equation, when $s=j\omega_0$, the loop gain $A(\omega_0)B(\omega_0)$ equal to -1, with finite $A(s)$, the close loop gain will reach infinity. Under this condition, a large output voltage can be got for an infinitesimally small input voltage. The negative feedback system changed to positive feedback and the oscillation starts.

In summary, a negative-feedback circuit has to satisfy following two conditions called “Barkhausen criteria”, and then the circuit may oscillate at ω_0 .

$$|A(j\omega_0)||B(j\omega_0)| \geq 1 \quad (5.2)$$

$$\angle A(j\omega_0)B(j\omega_0) = 180^\circ \quad (5.3)$$

In practical design, the magnitude of the close loop gain is typically chosen to be twice or three times the required value in order to ensure oscillation in the presence of temperature and process variation as well as the open loop gain decrease due to the circuit nonlinearity. And the phase shift requirement in “Barkhausen criteria” state a total phase shift of 360° . If the system is designed to have a low frequency negative feedback, $\angle A(j\omega_0)B(j\omega_0) = 180^\circ$ denotes additional frequency dependent phase shift as it already produces 180° of phase shift as represented by the subtractor. The “input signal” of the system here may be generated by any noise or fluctuation in oscillators.

The two port feedback model is very convenient for analyzing some types of oscillators such as ring oscillators. However, a LC-tank oscillator may get more insights into the oscillation phenomenon through the “negative resistance” concept.

5.1.3 One Port Negative Resistance Model of Oscillators

For an ideal LC resonator as shown in Fig. 5.2(a), it oscillates at the frequency $\omega_{res} = 1/\sqrt{LC}$. However, the real on chip inductor and capacitor will have parasitic resistance as modeled in Fig. 5.2 (b), where R_L and R_C are the parasitic resistance of inductor and capacitor, separately. For a narrow band of frequencies, Fig. 5.2 (b) can be converted to the parallel combination in Fig. 5.2 (c). L_P , C_P and R_P are the equivalent parallel inductance, capacitance and resistance after conversion.

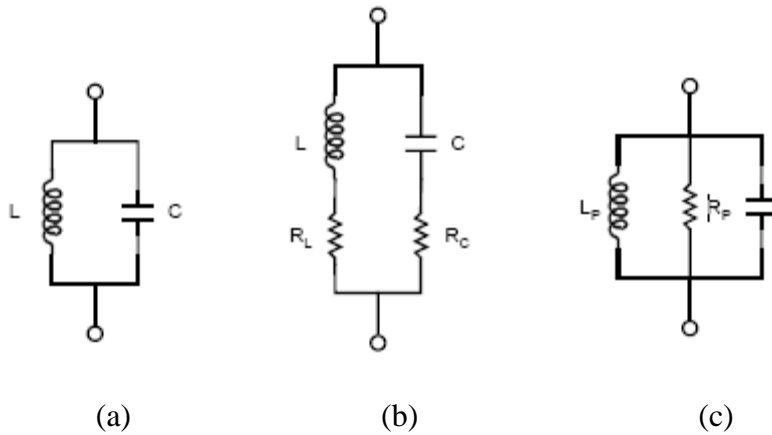
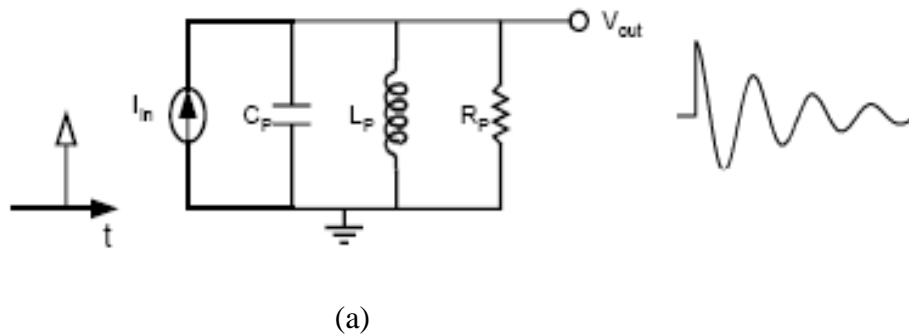
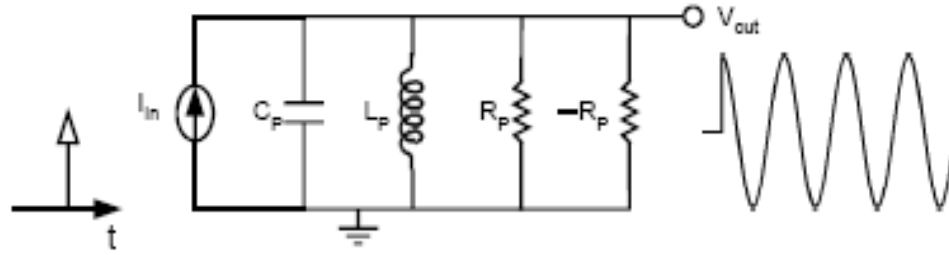


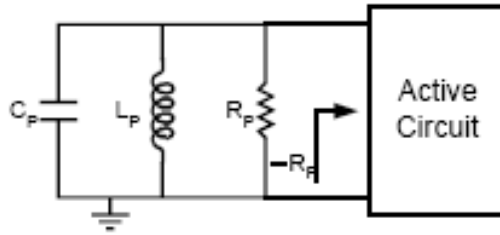
Figure 5.2 (a) Ideal LC resonator (b) practical LC resonator (c) LC resonator equivalent circuit

The concept of negative resistance model for oscillators can be explained in Fig. 5.3 [59]. In Fig. 5.3 (a), if a current impulse stimulates the tank, the circuit will respond with a decaying behavior because some of the stored energy is dissipated in the form of heat in R_P in every cycle. If an impedance $-R_P$ is placed in parallel with R_P , the equivalent parallel resistance seen by the lossless resonator is infinite. The energy lost in R_P is compensated by the negative resistance, allowing the steady oscillation. The negative resistance is usually provided by the active component in the circuit. Therefore, an oscillation circuit can be separated into two parts: one part is positive resistance which dissipates energy and another part is negative resistance which provides energy as shown in Fig. 5.3 (c).





(b)



(c)

Figure 5.3 Negative resistance model (a) decaying impulse response of a tank (b) addition of negative resistance to compensate loss in R_P (c) active circuit to provide negative resistance

5.2 Phase Noise

The most important characteristic for an oscillator is its frequency instability. For an ideal oscillator, the output in the frequency domain can be expressed as $V_{out} = A \cos(\omega_0 t + \varphi)$, where the amplitude A , oscillation frequency ω_0 and phase reference φ are all constants. The one side frequency spectrum of such an ideal oscillator is a single pulse centered at the output frequency ω_0 as shown in Fig. 5.4 (a). However, a practical oscillator cannot be ideal and is generally given as $V_{out} = A(t) \cos(\omega_0 t + \varphi(t))$, where $A(t)$ and $\varphi(t)$ are functions of time. As a consequence of the amplitude and phase fluctuation, the frequency spectrum of practical oscillator will contain noise sidebands close to the oscillation frequency ω_0 and its harmonics.

The frequency spectrum of a practical oscillator is shown in Fig. 5.4 (b). These sidebands are normally referring as phase noise sidebands [60].

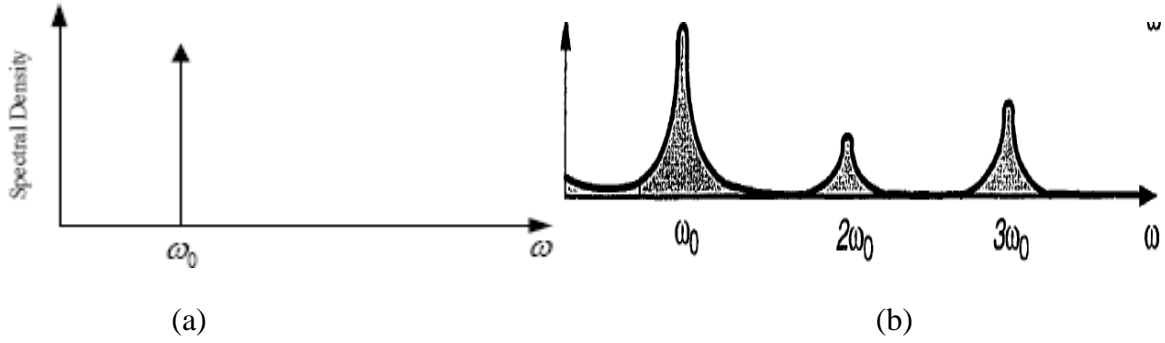


Figure 5.4 (a) Spectrum of an ideal oscillator (b) spectrum of a practical oscillator

One commonly used method to characterize the frequency instability of an oscillator is phase noise in the frequency domain viewpoint. Phase noise is usually characterized by single sideband noise spectral density. It can be expressed in equation 5.4.

$$L\{\Delta\omega\} = 10 \log \left(\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}} \right) \quad (5.4)$$

Where $\Delta\omega$ is the offset frequency, $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ is the single sideband noise power in a 1 Hz bandwidth at the offset frequency of $\Delta\omega$ from the carrier frequency ω_0 . $P_{carrier}$ is the carrier power. The unit of phase noise is decibels below carrier per Hz (dBc/Hz).

A typical phase noise of an oscillator in the function of offset frequency is shown in Fig. 5.5, where $\Delta\omega$ is shown on logarithmic scale. Three regions with different slopes are observed in the plot: $1/f^3$ region, $1/f^2$ region and flat region. At low offset frequency, the $1/f^3$ region has a negative slope of 30 dBc/decade. It is from the $1/f$ noise up conversion from various active devices [56].

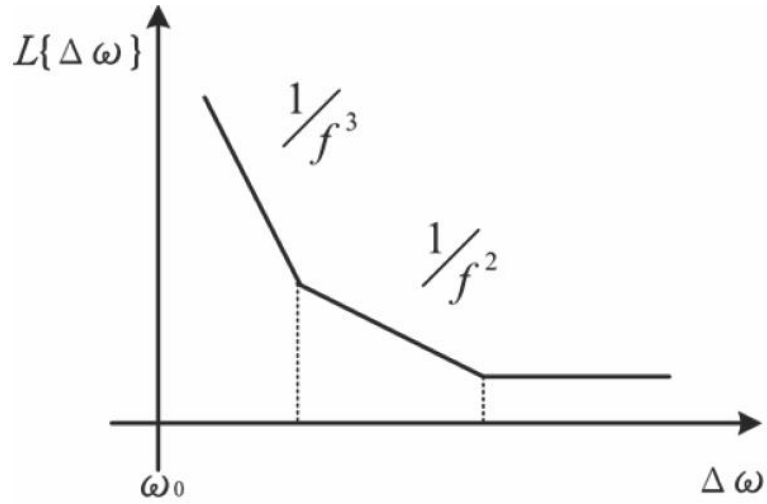


Figure 5.5 A typical phase noise plot

5.3 Voltage Controlled Oscillators (VCOs)

5.3.1 Mathematical Model of VCOs

The previous introduced oscillators work only at single frequency; however, many applications require that oscillators can work at certain tunable range. A voltage controlled oscillator is an oscillator where the output frequency is a function of a DC voltage. The output frequency of an ideal VCO is a linear function of its control voltage as shown in Fig. 5.6. It can be expressed in equation (5.5)

$$\omega_{out} = \omega_0 + K_{VCO}V_{cont} \quad (5.5)$$

Here, V_{cont} is the control voltage, ω_0 is the oscillation frequency at $V_{cont}=0$, and K_{VCO} represents the “gain” of the VCO.

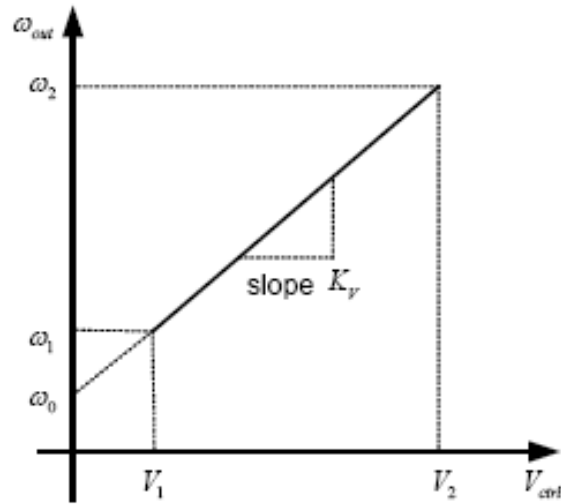


Figure 5.6 Characteristic of an ideal VCO

The important performance parameters of a VCO circuit design are center frequency (ω_{center}), tuning range, tuning gain (K_{VCO}), tuning linearity, output amplitude, power dissipation and output signal purity [61]. The required tuning range of a VCO is determined by the variation of the VCO center frequency with process and temperature and the frequency range necessary for the application. The tuning gain K_{VCO} is desired to be large for the tuning range, but on the other hand, large tuning gain makes the oscillator more sensitive to noise on the control line. The gain of an ideal oscillator is constant across the tuning range, however, the gain K_{VCO} of an actual oscillator is not constant, and the tuning characteristics of VCOs exhibit nonlinearity. It's desirable to minimize the variation of K_{VCO} across the tuning range. Large output oscillation amplitude is desirable to reduce the gain of the oscillator K_{VCO} thus can reduce the circuit's sensitivity to noise. And the power dissipation trades with phase noise and output amplitude.

5.3.2 Tuning in LC-tank Oscillators

The oscillation frequency of a LC resonator is expressed as $f_{osc} = 1/(2\pi\sqrt{LC})$, suggesting that the oscillation frequency is mainly determined by the inductor and capacitor values. Since it is difficult to change the value of the inductor, the tank capacitance is normally changed to tune the oscillator frequency. The voltage-dependent capacitors called “varactors” are usually implemented with PN junction diode or MOS capacitors while the MOS capacitors include normal-mode MOS capacitor, accumulation-mode capacitor and inversion-mode capacitor.

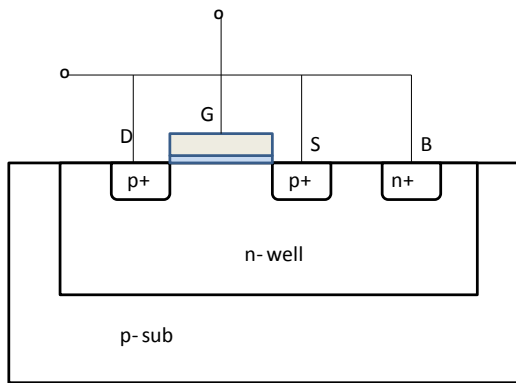
The PN junction varactor is formed by the P+ diffusion on an n-well. The operation of the PN junction varactors is based on the junction capacitance associated to the depletion region between the P+ diffusion and the Nwell [62]. Under reverse biased condition, the depletion width changes with the reverse bias voltage resulting in the total charges in the depletion region change. Thus the depletion capacitance changes with the controlled reverse bias voltage. One main disadvantage of the PN junction varactors is that they become forward biased with large amplitude voltage swings. The control voltage is typically limited to half the supply voltage to make sure the junction remain in reverse biased region to avoid Q degradation results in a small tuning range.

MOS varactors are implemented by biasing the MOS device in different working region to change the capacitance. Based on the different connections of drain, source and bulk, MOS varactors include normal-mode varactor, inversion-mode varactor and accumulation-mode varactor. The structures and C-V curves for the three types of MOS varactors are shown in Fig. 5.7. Each structure is a pMOS transistor in an n-well. pMOS is preferred because the bulk of an n-well can be biased at variable voltage [63][64].

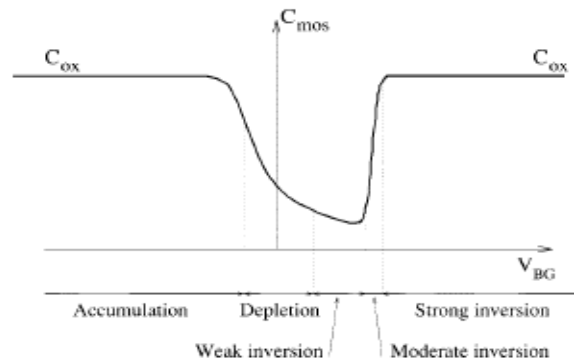
Fig. 5.7 (a) shows a pMOS with drain, source and bulk connected together forming a MOS capacitor that the capacitance value of the varactor is dependent on the voltage V_{BG} between bulk and gate. There are three operating conditions in the MOS capacitor: accumulation, depletion and inversion. When the bulk voltage is lower than the gate voltage, an accumulation layer of electrons is introduced at the oxide-semiconductor interface. A small differential change in voltage across the MOS structure will cause a differential change in charges on the metal gate and in the electron accumulation charges as in a parallel-plate capacitor. The value of the MOS capacitance is just the oxide capacitance. In the case of $V_{BG} > |V_{th}|$, an inversion layer is formed at the oxide-semiconductor interface. When $V_{BG} \gg |V_{th}|$, the transistor is in strong inversion where a small change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density that the capacitance is again the oxide capacitance. Therefore, in both strong inversion and accumulation region, the value of capacitance is equal to $C_{ox} = \epsilon_{ox}S/t_{ox}$, where t_{ox} is the oxide thickness and S is the transistor channel area. For intermediate value of V_{BG} , the MOS transistor works in depletion region, weak inversion and moderate inversion where the oxide capacitance and the capacitance of the depletion region are in series. The C-V characteristic curve of the MOS capacitor is shown in Fig. 5.7 (b). The tuning capability of the normal-mode varactor is limited by the nonmonotonicity of the capacitance.

If the bulk of the MOS device is connected to the highest voltage V_{dd} in the circuit, the MOS capacitor will work only in depletion and inversion region called inversion-mode MOS varactor. The structure and the C-V characteristic curve for an inversion-mode varactor are shown in Fig. 5.7 (c) and 5.7 (d), respectively.

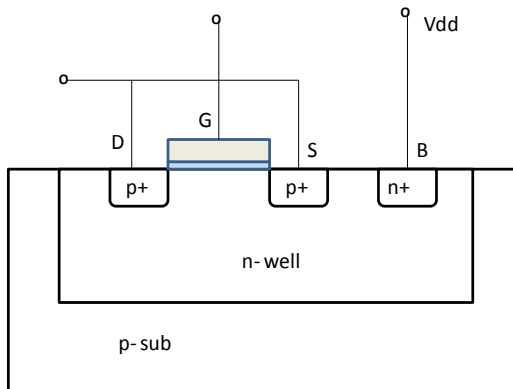
The structure of an accumulation-mode MOS capacitor is shown in Fig. 5.7 (e) which has two n+ regions in an n-well. The original source and drain region with P+ diffusion are replaced by n+ bulk contact. Such MOS capacitor only work in accumulation region and depletion region called accumulation-mode varactor. The C-V characteristic curve is shown in Fig. 5.7 (f).



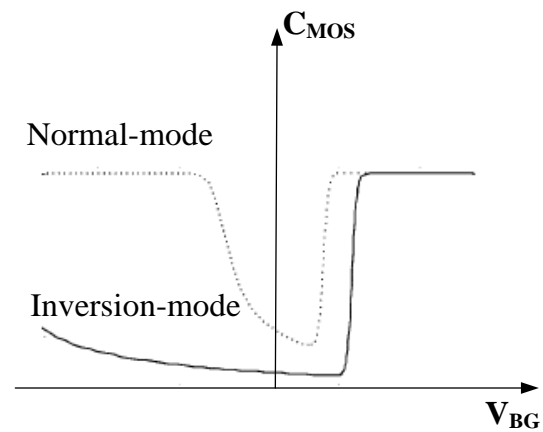
(a)



(b)



(c)



(d)

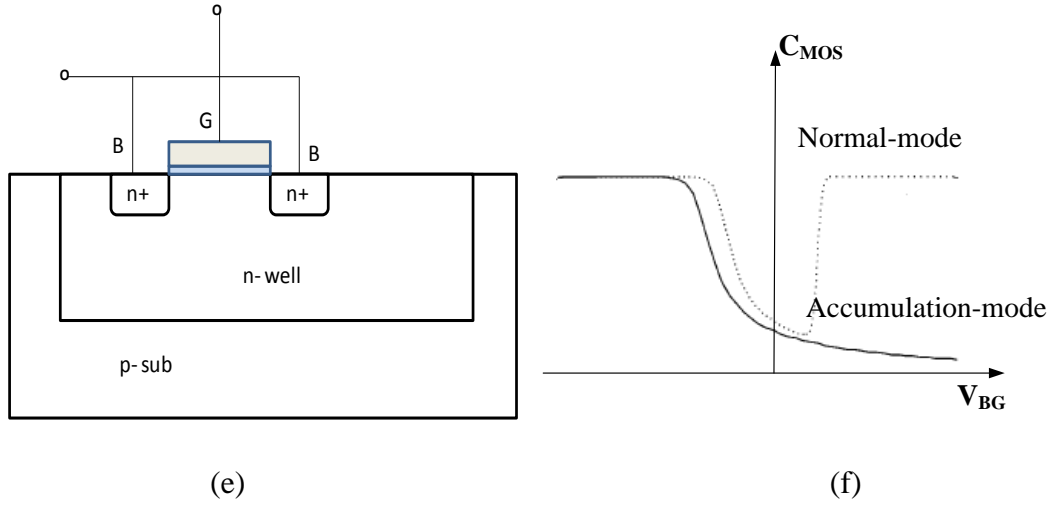


Figure 5.7 (a) Normal-mode MOS varactor structure (b) normal-mode MOS varactor C-V curve
(c) Inversion-mode MOS varactor structure (d) inversion-mode MOS varactor C-V curve (e)
accumulation-mode MOS varactor structure (f) accumulation-mode MOS varactor C-V curve

5.4 Injection Locking in Oscillators

Injection of a periodic signal into a free-running oscillator can lead to interesting non-linear phenomena. Suppose an input signal with frequency ω_i is applied to an oscillator with natural frequency ω_o , if ω_i is quite different from ω_o , “beat” of the two frequencies are observed. When ω_i enters some frequency range very close to ω_o , the output frequency of the oscillator is the same as that of the external signal instead of ω_o , the oscillator locks to this external signal. If the injected signal frequency lies out of, but not very far from the locking range, the oscillator is “pulled”. The injection locking have been known to exist for a long time back to the 17th century for the observation of locking phenomenon between two pendulums clocks [65]. Over the years, analysis of injection locking of oscillators has been studied by Adler [66], Kurokawa [67] and others [68-70].

The phase relationship between the injection signal and the injection locked signal can be approximated by Adler's equation [66] which is in the form of a non-linear differential equation and can also be used to find the locking range. The oscillator is modeled as a feedback system with a resonator as shown in Fig. 5.8 [71]. The injection signal E_{inj} is added to the oscillator output signal E_{osc} in the feedback path and the total signal is E_T . Fig. 5.9 represent the voltage vectors of the signals in Fig. 5.8 at a given instant during the beat cycle.

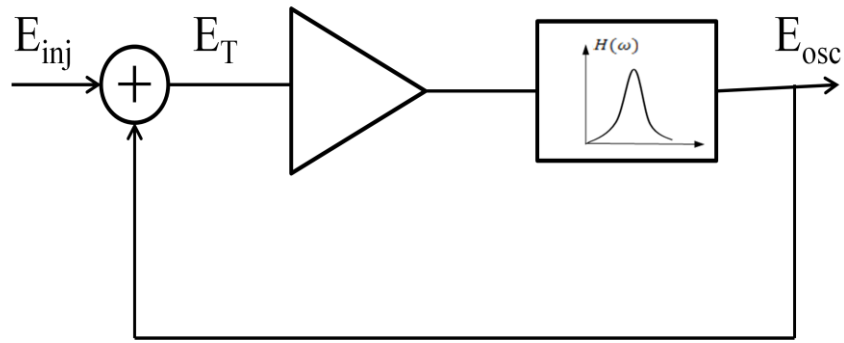


Figure 5.8 Injection locked oscillator model

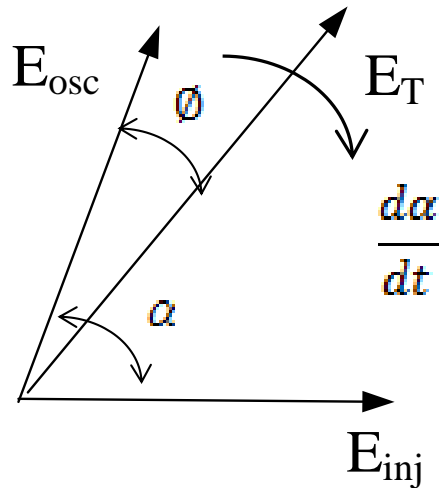


Figure 5.9 Vector diagram of signals in Fig. 5.8

With no injection signal applied, E_T and E_{osc} are aligned at the free running frequency ω_o . When an external voltage E_{inj} is introduced, E_T is no long in phase with E_{osc} . Assume $E_{inj} \ll E_{osc}$ yields:

$$\phi = \frac{E_{inj}}{E_{osc}} \sin \alpha \quad (5.6)$$

The phase-frequency relation for a single tuned circuit in the vicinity of the free-running frequency is given by:

$$\tan \phi = 2Q \frac{\omega - \omega_o}{\omega_o} \quad (5.7)$$

For small frequency deviation $\frac{\omega - \omega_o}{\omega_o} \ll 1$:

$$\phi = \arctan \left(2Q \frac{\omega - \omega_o}{\omega_o} \right) = 2Q \frac{\omega - \omega_o}{\omega_o} \quad (5.8)$$

The instantaneous beat frequency can be written as

$$\frac{d\alpha}{dt} = \omega - \omega_{inj} = (\omega - \omega_o) + (\omega_o - \omega_{inj}) = (\omega - \omega_o) + \Delta\omega_o \quad (5.9)$$

From equation (5.6), (5.8) and (5.9), therefore”

$$\frac{d\alpha}{dt} = \frac{E_{inj}}{E_{osc}} \frac{\omega_o}{2Q} \sin \alpha + \Delta\omega_o \quad (5.10)$$

At steady state, when injection locking occurs, $\frac{d\alpha}{dt} = 0$. The phase difference between give the injection signal and the oscillation signal is given by

$$\sin \alpha = 2Q \frac{E_{osc}}{E_{inj}} \frac{\Delta\omega_o}{\omega_o} \quad (5.11)$$

Since $|\sin \alpha| < 1$, therefore

$$\left| \frac{\Delta\omega_o}{\omega_o} \right| < \frac{1}{2Q} \cdot \frac{E_{inj}}{E_{osc}} \quad (5.12)$$

The locking range can be obtained as:

$$\omega_L = \frac{\omega}{2Q} \cdot \frac{E_{inj}}{E_{osc}} \quad (5.13)$$

Thus the locking range is proportional to the injection signal amplitude E_{inj} and inversely proportional to the quality factor Q and the oscillation amplitude E_{osc} .

Adler's equation is get for a special case by assuming $E_{inj} \ll E_{osc}$. The general expression for locking range without assuming the small injection is derived with the similar procedure in [68] and [70] as below:

$$\omega_L = \frac{\omega}{2Q} \cdot \frac{E_{inj}}{E_{osc}} \frac{1}{\sqrt{1 - \frac{E_{inj}^2}{E_{osc}^2}}} \quad (5.14)$$

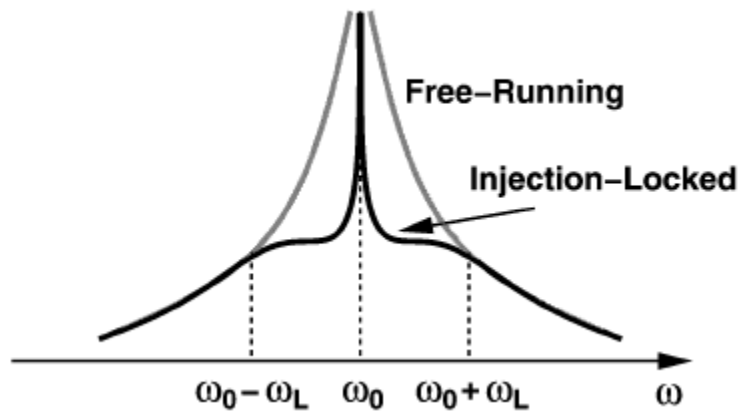


Figure 5.10 Phase noise of injection locked oscillator

By injection a low-noise source into the oscillation, the phase noise of injection-locked oscillators can be reduced. The phase noise of a free-running oscillator and an injection-locked

oscillator is shown in Fig. 5.10 [70], where ω_0 is the center frequency, ω_L is the locking range. For the injection frequency during the locking range, $\omega_0 - \omega_L < \omega_{inj} < \omega_0 + \omega_L$, the phase noise of the injection locked oscillator is much lower than that of the free-running oscillator. As the injection frequency deviates from the center of the locking range, the improvement of phase noise decreases. When the injection frequency reaches the edge of the locking range, the phase noise is increased to the level of free-running oscillator.

CHAPTER 6 : OSCILLATOR PHASE NOISE IMPROVEMENT USING INJECTION LOCK

6.1 Direct Injection Locked Oscillator

In this section, oscillators with two different injection locking schemes which are tail injection locking and direct injection locking are presented to achieve low phase noise oscillators.

Fig. 6.1 is the schematic of the direct injection locked oscillator used for simulation in ADS. Transistors M1 and M2 are used to provide negative resistances for the oscillator to cancel the resistive loss in the LC tank circuit. Transistor M3 is used as tail current source and the incident signal is injected into the oscillator through M4. Inductors L1 and L2 are connected with the drains of the cross-coupled transconductance transistors M1 and M2. L1, L2 and the varactors comprise the LC tank. The oscillator is designed in TSMC 0.18 um CMOS technology. The supply voltage V_{DD} is 1.5 V. The performances of the oscillator are simulated in ADS.

The free running frequency of the oscillator is 2.341 GHz from the ADS simulation at $V_{DD} = 1.5$ V and $V_{tune} = 1.5$ V. When the incident signal injected into the transistor M4 with proper amplitude and frequency, the output frequency of the injection locked oscillator will be locked to the frequency of the injection signal. The waveforms of the injection locked oscillator's differential output signal and the ac injection signal are shown in Fig. 6.2. Assume the free-running frequency of the oscillator and the input frequency are f_o and f_i , respectively. Under injection locked condition, when the injector is turned off, the voltages of the differential outputs become equal by $1/2f_o$ cycles. When the injector is turned on periodically by $1/f_i$ cycles, the voltages of differential outputs are equalized at the same time. There is one peak differential output voltage between the two peak injection signal voltages. Thus, the output oscillates by

$1/f_o$ cycles with $f_o = 1/(2f_i)$ and the circuit operates as a divide-by-two circuit. [72] As shown in Fig. 6.3, the oscillator's output frequency follows the injection frequency and it's half of that.

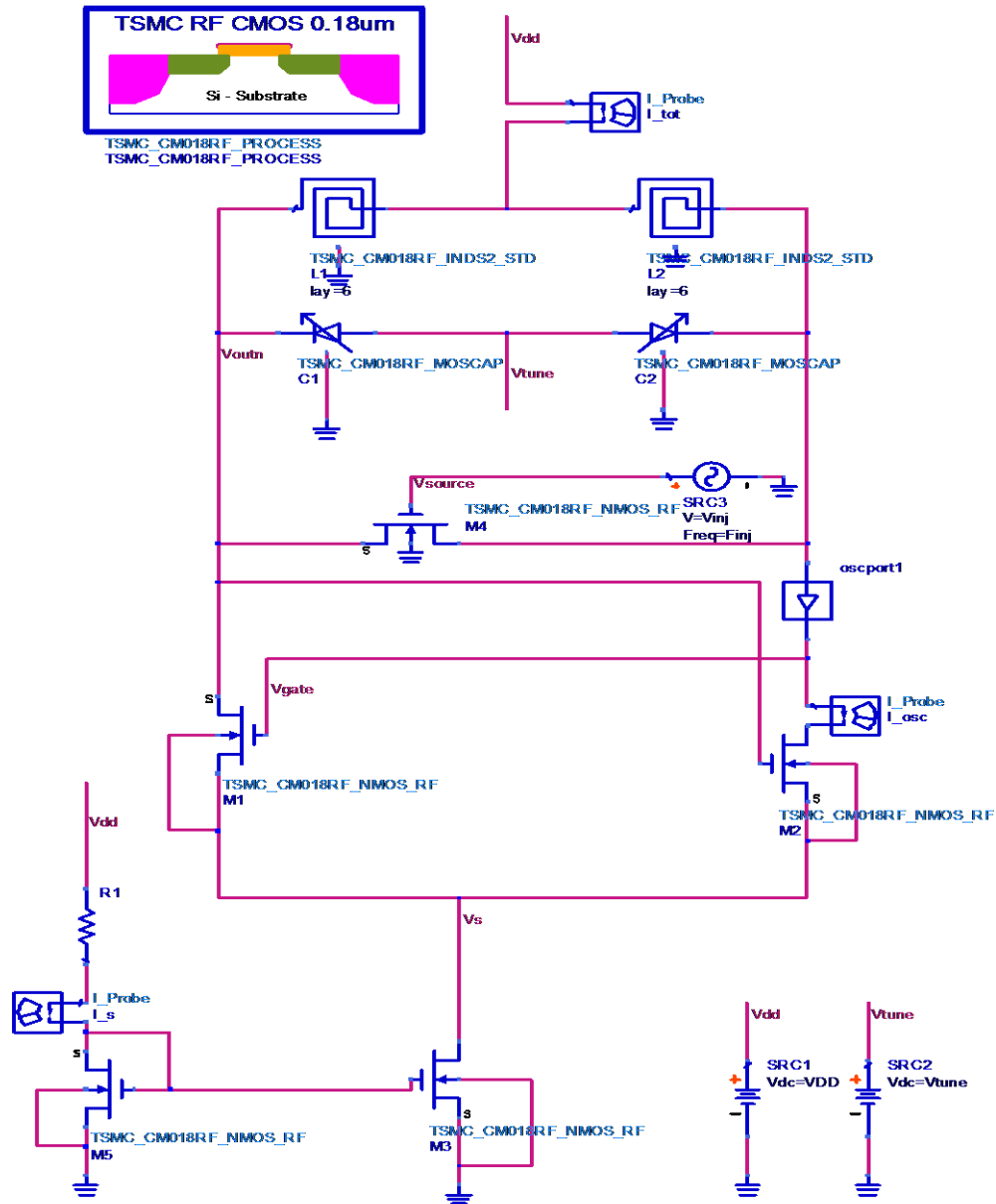


Figure 6.1 Schematic of the direct injection locked oscillator

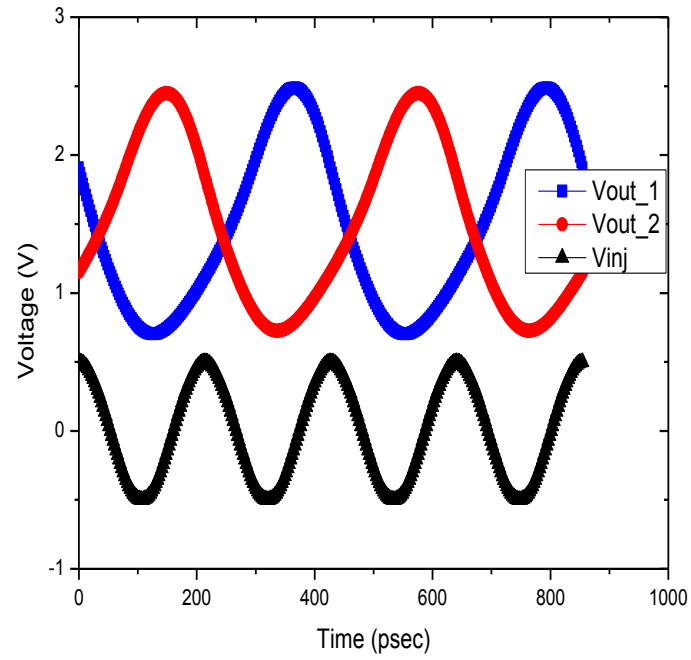


Figure 6.2 Waveforms of injection signal and the output voltage of the injection locked oscillator

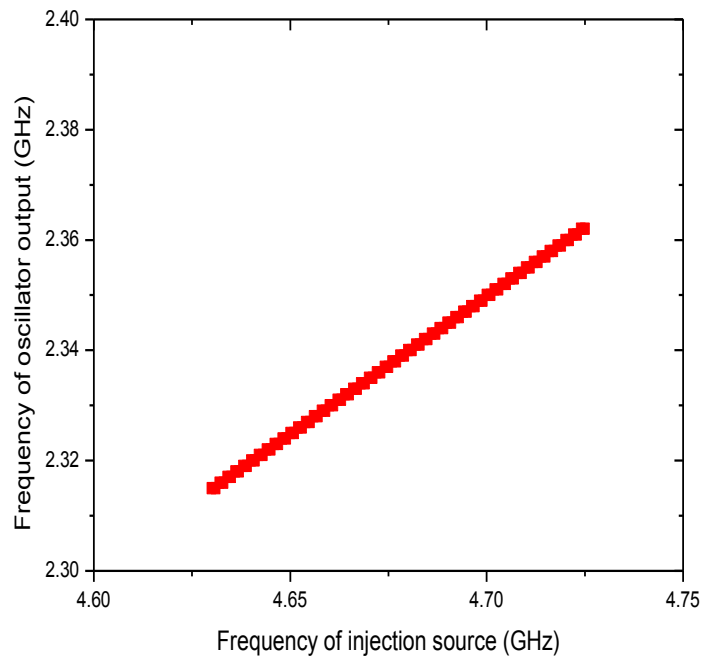


Figure 6.3 Output frequency versus injection frequency

Fig. 6.4 shows the simulated phase noise of the free-running oscillator, injection locked oscillator and the injection source. The phase noise of free-running oscillator is -120.1 dBc/Hz at 1 MHz offset frequency from the carrier. The phase noise of the injection locked oscillator is -140.8 dBc/Hz at 1 MHz when the injection signal is with amplitude of 0.5 V and with the phase noise of -133 dBc/Hz. The phase noise of the injection-locked oscillator is 20.7 dB lower than the phase noise of the free-running oscillator and 7.8 dB lower than that of the input signal at 1 MHz offset frequency from the carrier. The phase noise of the injection-locked oscillator tracks the low-phase-noise injection source and has significant improvement over that of the free-running oscillator. Thus, the phase noise of oscillator can be reduced by injection a low-noise source into the oscillator.

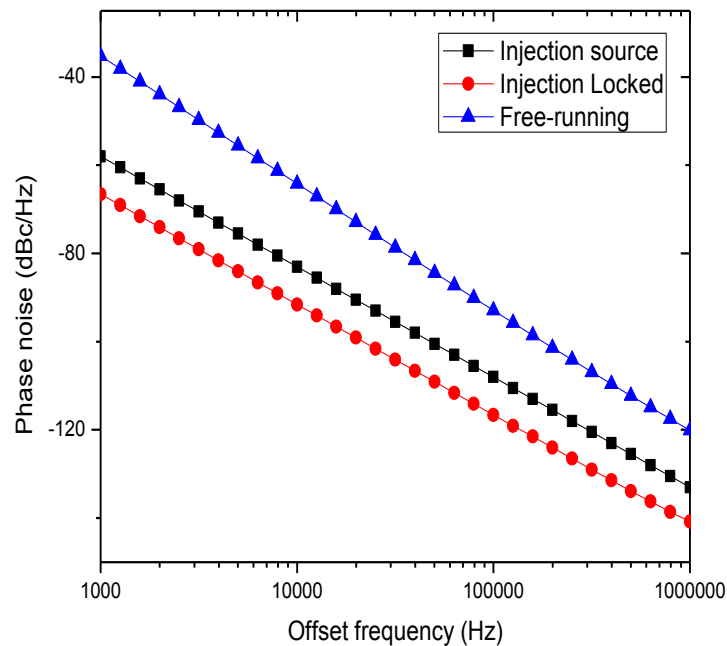


Figure 6.4 Simulated phase noise of the injection locked oscillator and the injection source

Fig. 6.5 shows the phase noise of the injection locked oscillator at 1 MHz offset frequency from the carrier in the function of the injection signal frequency with the amplitude of injection signal at 0.3 V, 0.5 V and 1 V. When the injection frequency is at the center of the locking range, the phase noise of the injection locked oscillator is around -140 dBc/Hz at 1 MHz offset frequency from the carrier which has significant improvement than that of the free-running oscillator. As illustrated in Fig. 6.5, if the input frequency deviates from the locking center, the phase noise reduction becomes less pronounced. As the input frequency approaches the edge of the locking range, the phase noise is increased to the level of free-running oscillator. As predicted by equation (5.13) that the locking range is proportional to the incident signal amplitude. The oscillator with injection signal level of 1 V has wider locking range than that with injection signal level of 0.3 V.

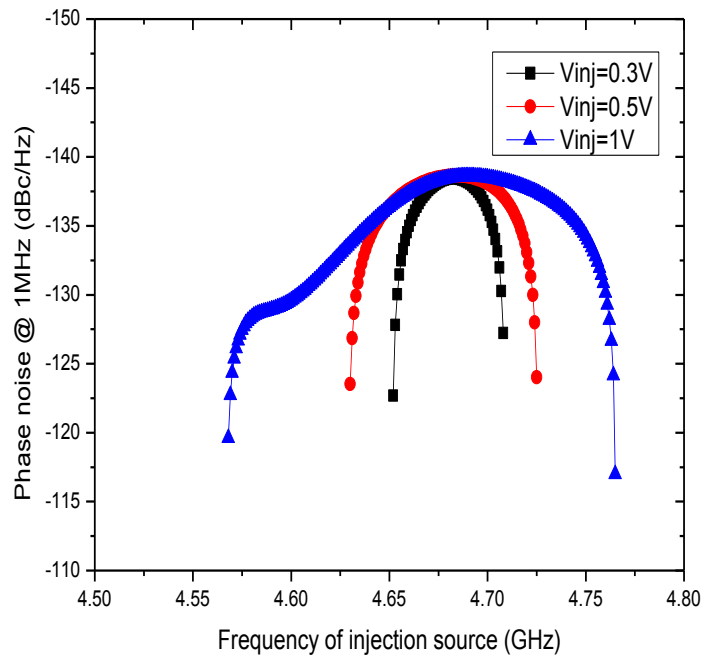


Figure 6.5 Phase noise in the locking range for different injection signal level

The summary of the locking range regarding to the injection signal amplitude is given in table 6.1. At $V_{DD} = 1.5$ V and $V_{tune} = 1.5$ V, a input signal with amplitude of 0.5 V can provide injection lock from 4.63 GHz to 4.725 GHz. Assuming f_{min} is the minimum operating frequency and f_{max} is the maximum operating frequency, the relative locking range can be defined as $f_R = \frac{f_{max}-f_{min}}{(f_{max}+f_{min})/2}$. The f_R is 4.22% for the injected signal with amplitude of 1 V and 1.2% for the injected signal with amplitude of 0.3 V.

Table 6.1 Locking range for different injection source

Amplitude of injection source	f_inj_min	f_inj_max	f_osc_min	f_osc_max	Locking range	Locking range
V	GHz	GHz	GHz	GHz	GHz	%
0.3	4.652	4.708	2.326	2.354	0.028	1.20%
0.5	4.63	4.725	2.315	2.3625	0.0475	2.03%
1	4.568	4.765	2.284	2.3825	0.0985	4.22%

6.2 Tail Injection Locked Oscillator

The schematic of the tail injection locked oscillator is shown in Fig. 6.6. The oscillator is designed with TSMC 0.18 μm CMOS technology and the supply voltage is 1.5 V. Inductors L1, L2 and varactors C1, C2 form the LC tank. Transistors M1 and M2 provide negative resistance for the oscillator. The incident signal is injected through the gate of the tail transistor M3. The free-running frequency of the proposed oscillator operates at 2.45 GHz when the tuning voltage is 1.5 V.

Fig. 6.7 shows the waveform of the injection signal and the output signals of the injection locked oscillator. The injection signal frequency is 4.9 GHz and the output frequency of the injection locked oscillator is 2.45 GHz. When the injection signal is injected through the gate of the tail transistor M3, it is delivered to the common source of the transconductance transistors M1 and M2. The output signals are feedback to the gates of M1 and M2. Thus the output signals and incident signal are summed across the gates and sources of M1 and M2. The common source connection of M1 and M2 oscillated at twice the frequency of the output signals. Under the injection locked condition, the output frequency of the injection locked oscillator is half of the frequency of the injection signal. Fig. 6.8 shows the relationship between incident frequency and output frequency in the locking range. Here, the amplitude of injection signal is 0.5 V. For the injection frequency changing from 4.823 GHz to 4.951 GHz, the output frequency of the injection locked oscillator is from 2.4115 GHz to 2.4755 GHz. The output frequency is half of the injection frequency as discussed above.

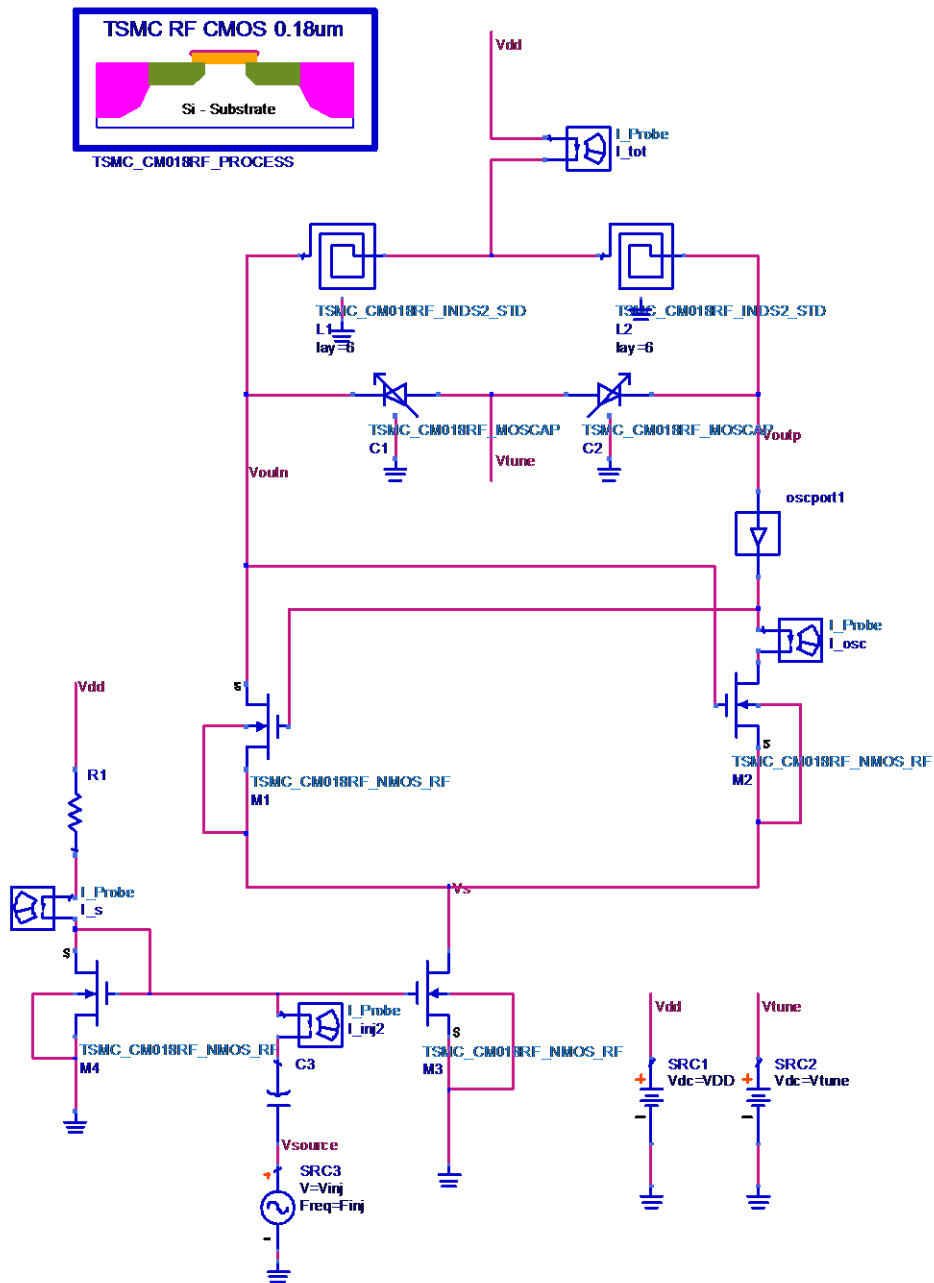


Figure 6.6 Schematic of the tail injection locked oscillator

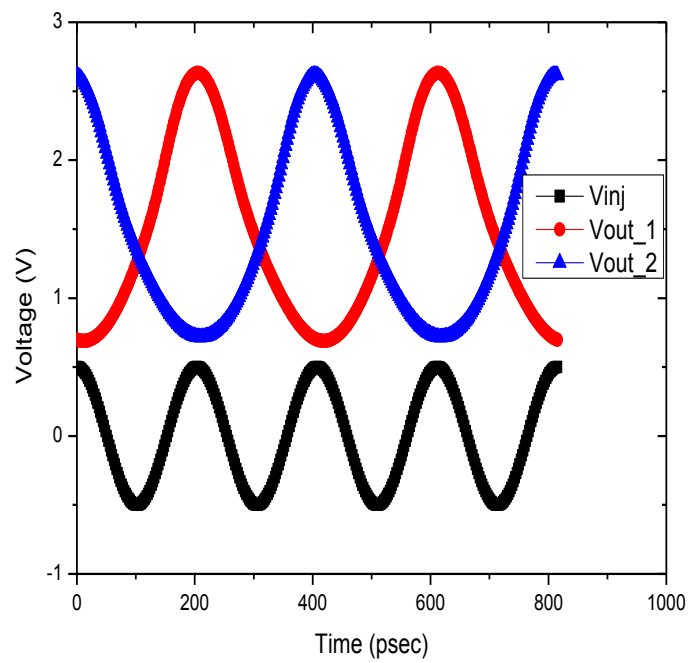


Figure 6.7 Waveforms of the injection signal and the output signals of the oscillator

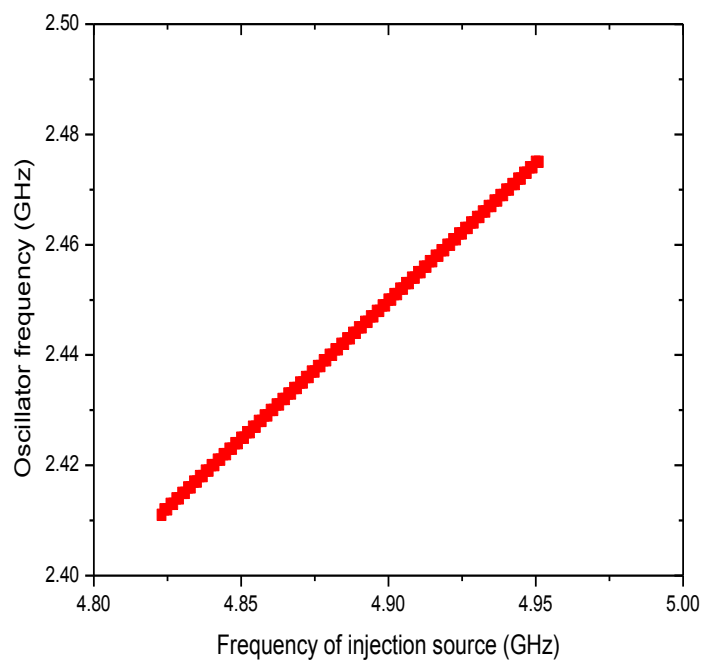


Figure 6.8 Frequency of the ILO versus the frequency of the injection signal

Simulated phase noise results are shown in Fig 6.9. The blue dot line is the phase noise of the free-running oscillator when there is no injection signal injected to the oscillator. The black dot line is the phase noise of the low-phase-noise injection source with amplitude of 0.5 V. The red dot line is the phase noise of the injection locked oscillator. The phase noise at 1 MHz offset frequency from the carrier for the free-running, injection source and injection locked oscillator is -118.5 dBc/Hz, -133 dBc/Hz and -138.4 dBc/Hz, respectively. The phase noise of injection locked oscillator is 19.9 dB lower than the phase noise of the free running oscillator and 5.4 dB lower than that of the input signal at 1 MHz offset frequency from the carrier.

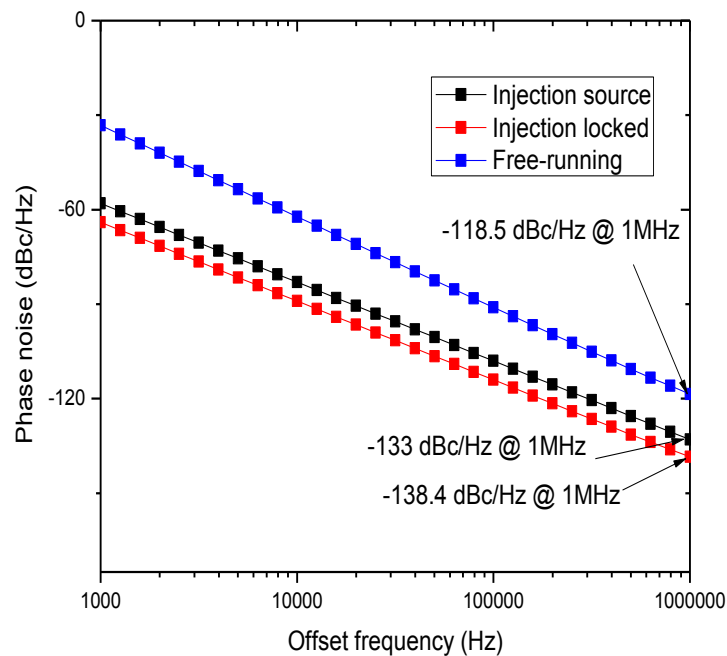


Figure 6.9 Phase noise of the free-running, injection source and the injection locked oscillator

Fig. 6.10 shows the phase noise of the injection locked oscillator as a function of the incident frequency for different incident amplitude at 1 MHz offset frequency from the carrier.

The locking range is determined by the frequency difference between the two ends of each curve. At the center of the locking range, the phase noise of the injection locked oscillator is around -138 dBc/Hz, which is about -19 dB improvement compared to the free-running oscillator. As the injection frequency deviates from the center of the locking range, the improvement of phase noise reduces. At the edge of the locking range, the phase noise is increased to the level of free-running oscillator. Also, the locking range of the oscillator increases with the increase of incident amplitude.

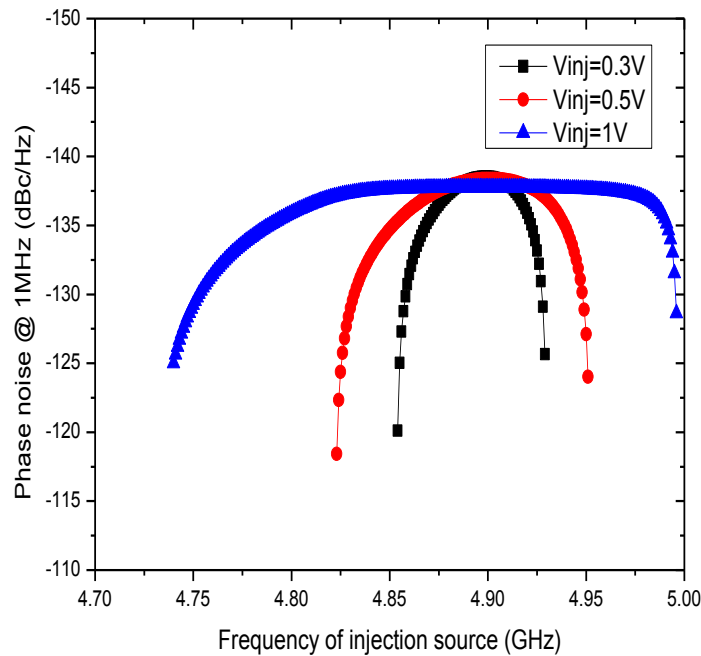


Figure 6.10 Phase noise in locking range for different injection amplitude

An alternate way to investigate the locking range is to monitor the output amplitude of the oscillator. Fig. 6.11 shows the oscillation amplitude of the injection locked oscillator as a function of the incident frequency for different incident amplitude. The oscillation amplitude

decreases as the injection frequency get close to the locking range which explains the high phase noise of the injection locking

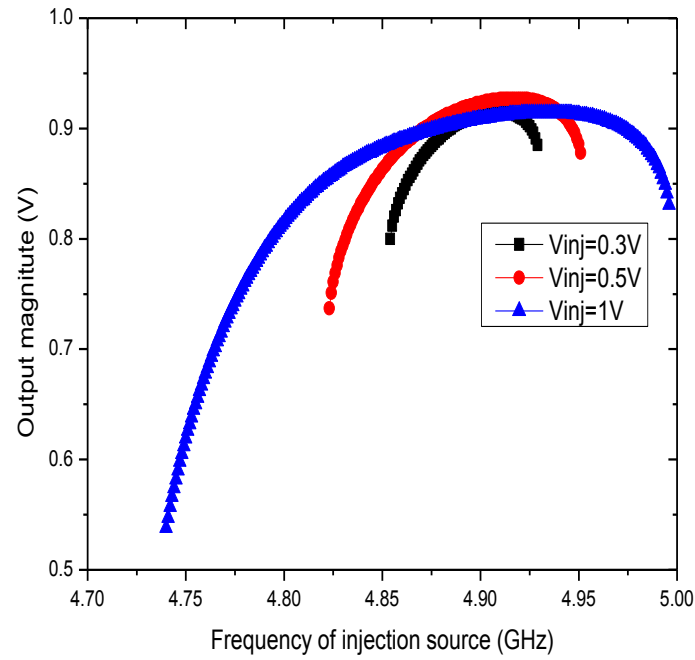


Figure 6.11 Oscillation output amplitude of the injection locked oscillator

Table 6.2 Summary of tuning range for tail injection locked oscillator

Magnitude of injection source	f_inj_min	f_inj_max	f_osc_min	f_osc_max	Locking range	Locking range
V	GHz	GHz	GHz	GHz	GHz	%
0.3	4.854	4.929	2.427	2.4645	0.0375	1.53%
0.5	4.823	4.951	2.4115	2.4755	0.064	2.62%
1	4.74	4.996	2.37	2.498	0.128	5.26%

The locking range for different injection signal amplitude is summarized in table 6.2. At $V_{DD} = 1.5$ V and $V_{tune} = 1.5$ V, the locking range for an input signal with 0.3 V is 37.5 MHz which is 1.53% of the center frequency. By increasing the incident amplitude to 1 V, the locking range increases to 128 MHz which is 5.26% of the center frequency.

CHAPTER 7 : REALIABILITY STUDY OF A FULLY DIFFERENTIAL CLAPP-VCO

Due to aggressive scaling in device dimensions for improving speed and functionality, the channel electric field becomes higher and hot electron effect becomes more significant[9],[73]. The hot carrier injection introduced interface traps and oxide trapped charges can cause device performance drifts of threshold voltage and transconductance. Even at low supply voltage, degradation effects caused by hot carriers have been observed. Hot carrier effect can also degrade RF circuit performance [74]-[76].

Voltage controlled oscillator is the most important circuit block in modern RF communication systems and is used for generating the intermediate frequency signal and modulate or demodulating the RF signal. It's desirable for a VCO to have low phase noise, wide tuning range and high stability. However, the VCO performance is very sensitive to the variation of device parameter. It's been reported that the phase noise increases and tuning range decreases after hot electron effect [75][76]. However, the previous publications for VCOs degradations were evaluated under DC stress. In practical, the VCOs are operating under large-signal RF excitation.

In this section, the reliability of a differential clap-VCO subject to large-signal RF stress has been investigated.

7.1 Circuit Design

The schematic of the differential Clapp-VCO used for hot carrier stress experiment is shown in Fig. 7.1 [77]. It's modified from the differential Colpitts VCO using parallel-tuned

resonator [78] to a series-tuned resonator. The main part of the LC tank consists of varactors (C_{var}) and inductors L_0 and L_1 . The inductors are constructed as a symmetric inductor to enhance the Q-factor of resonator, save die area and also enhance differential mode operation. C_{var} are the accumulation-mode MOS varactors used to tune the operation frequency of the oscillator. The resistors R are used for gate bias. V_{Bias} provides the gate bias for transistor M_2 and M_3 . M_2 and M_3 are used to provide negative resistances for the VCO core to cancel the resistive loss in the LC tank circuit. Two cross-coupled transistors M_1 are self-biased and mainly used as the current source. They also provide additional negative resistance of the oscillator. The channel length for the four nMOSFETs is 0.13 μm .

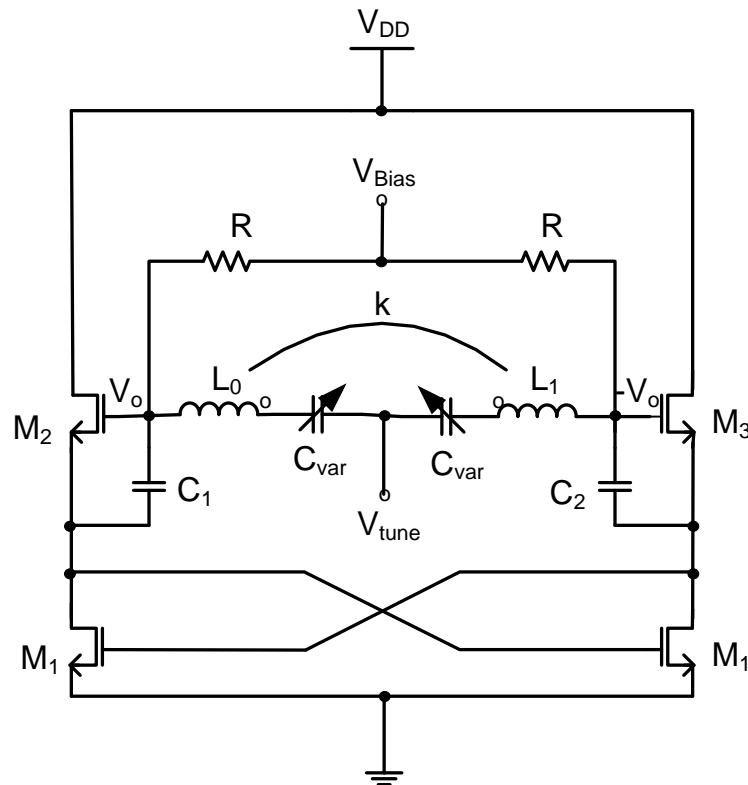


Figure 7.1 Schematic of the differential Clapp-VCO

The frequency of the oscillator is approximated by [77]

$$f_{osc} = \frac{1}{2\pi} \left[\frac{1}{L} \left(\frac{1}{C_{var}} + \frac{1}{C_{act}} \right) \right]^{1/2} \quad (7.1)$$

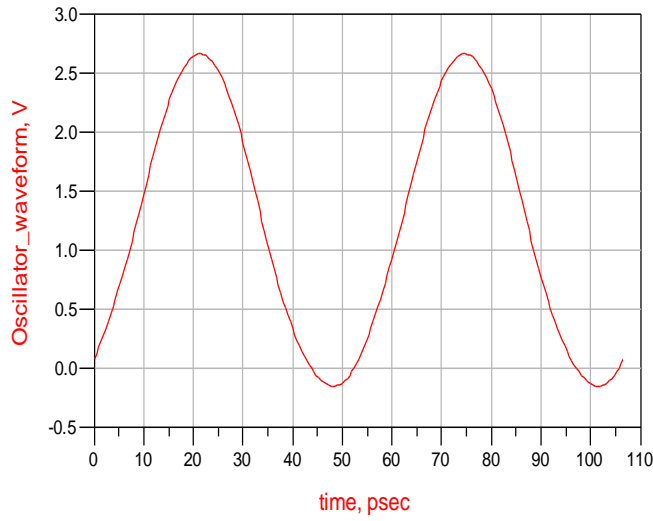
Where C_{var} is the varactor capacitance, and C_{act} is the net capacitance from $C_1, C_{gs1}, C_{gs2}, C_{ds1}$ and C_{ds2} , where C_{gsi} and C_{dsi} ($i = 1, 2$) are the gate source capacitances and gate drain capacitances, respectively. L is the inductor of the resonator tank.

The condition for oscillation is that the negative input resistance at least compensates for resonator losses at oscillation frequency.

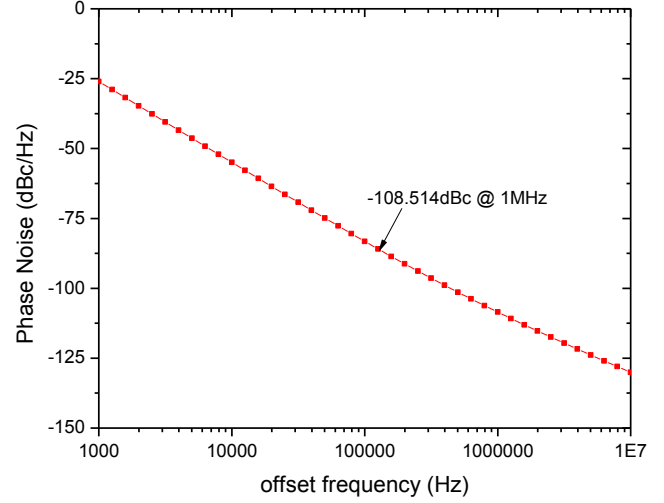
$$R_{acrt} + R_{res} < 0 \quad (7.2)$$

Where R_{res} is the parasitic resistance of the series-resonator, and R_{acrt} is the negative resistance from the active devices.

The oscillator is designed and simulated in ADS. Fig. 7.2 (a) and (b) are the simulated oscillation waveform and phase noise curve of the oscillator. The supply voltage is 0.9 V. The phase noise is -108.514 dBc/Hz at 1 MHz offset frequency.



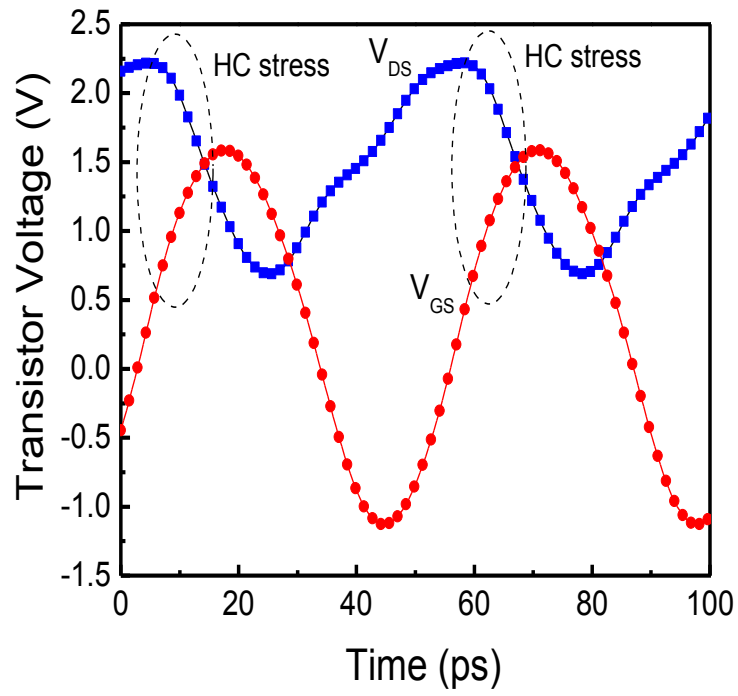
(a)



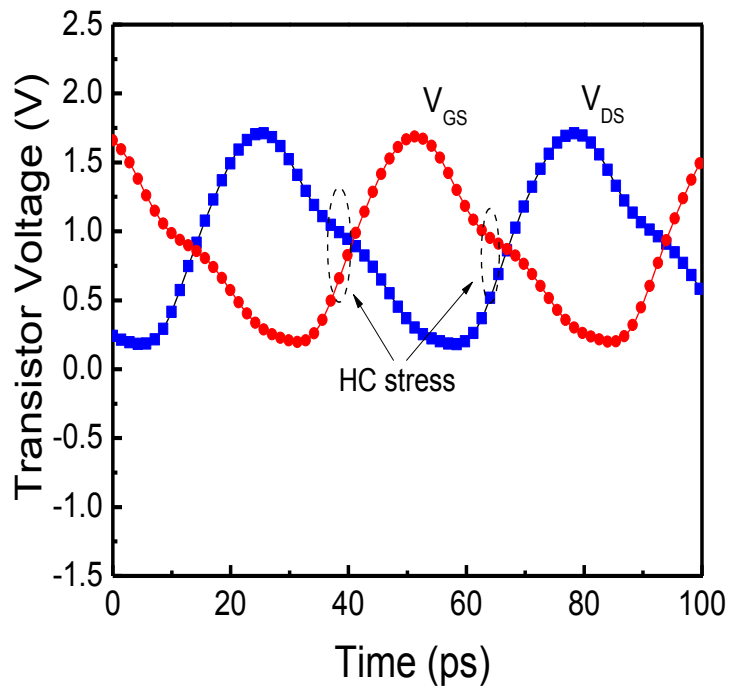
(b)

Figure 7.2 (a) Oscillator output waveform (b) phase noise versus offset frequency

Fig. 7.3 (a) and (b) show the drain-source voltage and the gate-source voltage of the negative transconductance transistor M2 and the current source transistor M1 during the transient operation from ADS circuit simulation, respectively. In Fig. 7.3 (a), when V_{GS} for transistor M2 is above its threshold voltage, V_{DS} is at large value suffering severe hot electron RF stress during switching. While in Fig. 7.3 (b), when V_{GS} for transistor M1 is above its threshold voltage, V_{DS} is at the low value portion of its cycle. The hot electron RF stress on the current source transistor M1 is much less than that of the transconductance transistor M2.



(a)



(b)

Figure 7.3 (a) Simulated V_{GS} and V_{DS} on M2 (b) Simulated V_{GS} and V_{DS} on M1

7.2 RF Stress Experiments

Fig. 7.4 shows the photograph of the fabricated VCO [77]. The total chip area is $0.931 \times 0.606 \text{ mm}^2$ including all RF and DC test pads and dummy metals. The two inductors are configured as an octagonal two-turn transformer. The circuit is biased at the supply voltage of 0.9 V.

The oscillator's performances before and after RF stress are measured with an Agilent E5052 Signal Source Analyzer at room temperature. The differential Clapp-VCO was stressed under the continued RF large-signal transient condition with an elevated supply voltage of 2.4 V for 10 hours. After 10 hours of RF stress, the oscillator's performances were measured at the normal circuit bias of V_{DD} at 0.9 V.

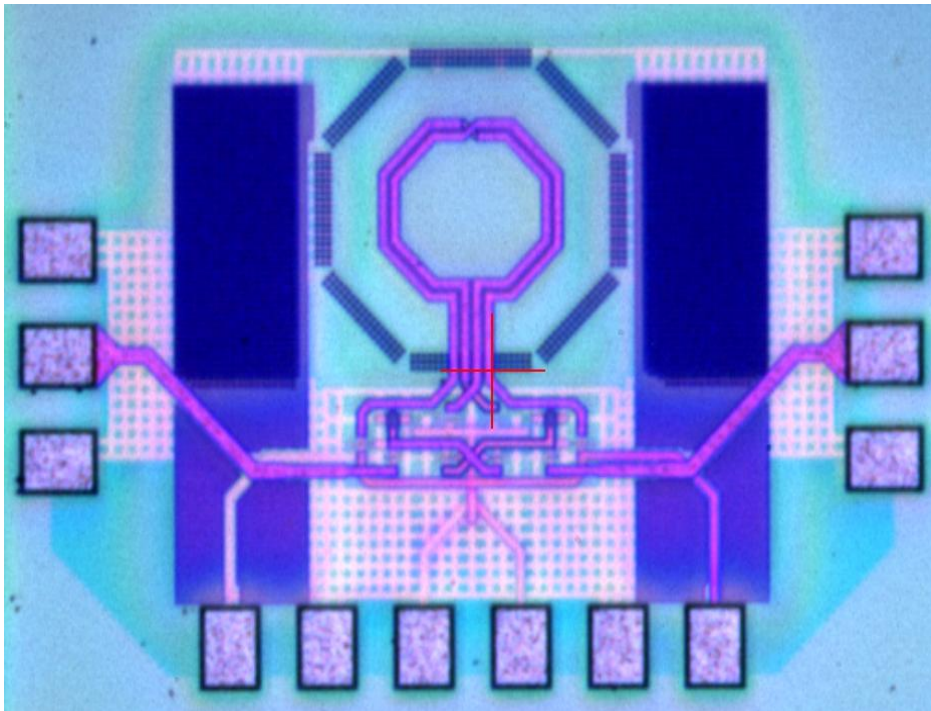


Figure 7.4 Microphotograph of the fabricated chip

The output current of the differential Clapp-VCO was monitored before and after the RF stress. For the fresh circuit, the drain current of the transconductance transistor is about 6 mA at $V_{\text{tune}} = 0$ V. After the Clapp-VCO was stressed for 10 hours, the drain current of the transconductance transistor decreases to 5.13 mA at $V_{\text{tune}} = 0$ V. As shown in Fig. 7.3 (a), the transconductance transistor experiences severe hot electron stress under the continued RF large-signal transient condition. The hot electron injection increases the threshold voltage and decreases the mobility of the MOSFET resulting in the decrease of the drain current of the transconductance transistor.

Fig. 7.5 shows the measured oscillation frequency in the function of the tuning voltage before and after the RF stress. The red line represents the fresh circuit and the blue line represents the circuit after 10 hours of RF stress. As the tuning voltage sweeps from 0 V to 1.3 V, the varactor's capacitance decreases thus the oscillation frequency increases. At the fresh condition, the tuning range is from 18.8 GHz to 22.2 GHz when the tuning voltage changes from 0 V to 1.3 V. After 10 hours of RF stress, the gate-drain capacitance of the transistor decreases and the gate-source capacitance increases as a result of hot electron stress [79]. The decrease of gate-drain capacitance is more than the increase of gate-source capacitance. Thus, the effective total capacitance of the resonant circuit decreases after hot electron degradation resulting in the increase of the oscillation frequency. As shown in Fig. 7.5, at the tuning voltage of 1.2 V, the oscillation frequency is 22.2 GHz at fresh condition while it's 22.6 GHz after 10 hours of RF stress. The oscillation frequency increases after RF and V_{DD} stresses.

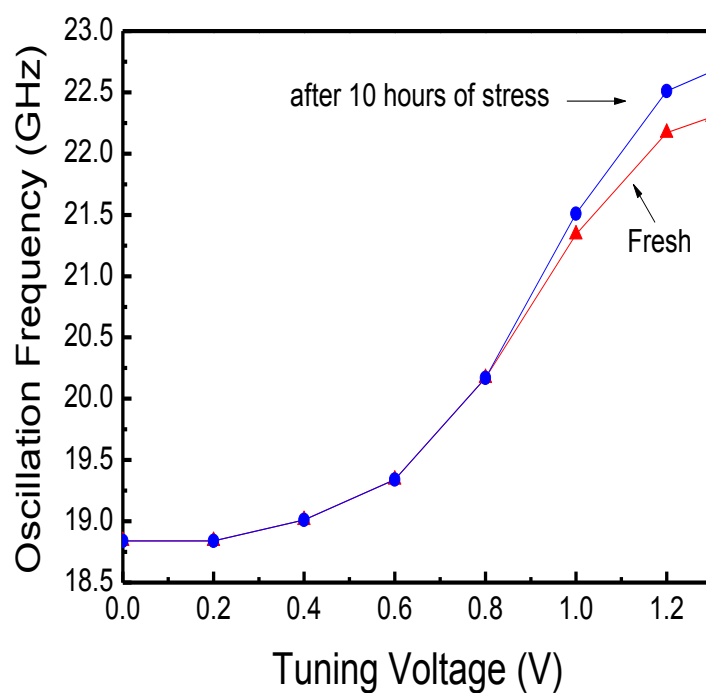


Figure 7.5 Measured oscillation frequency versus tuning voltage before and after RF stress

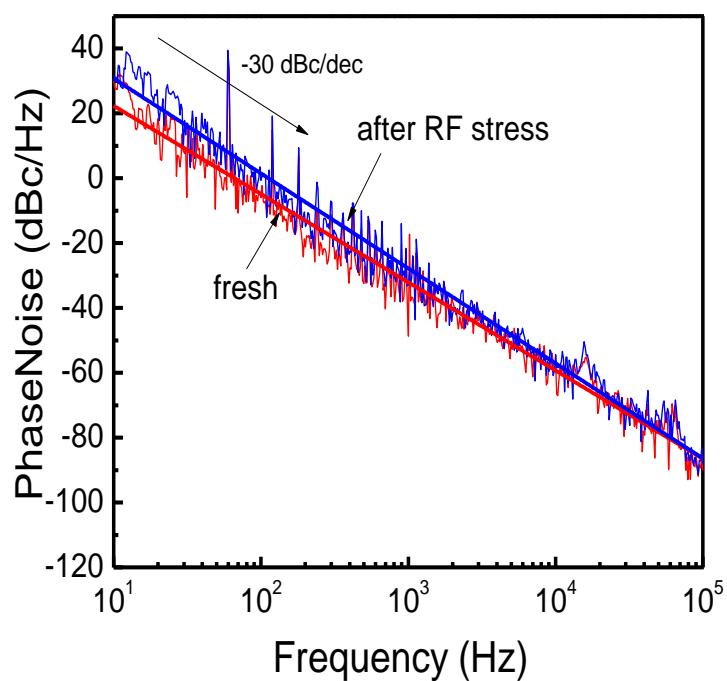


Figure 7.6 Measured phase noise versus offset frequency before and after RF stress

The phase noise of the Clapp-VCO before and after RF stress is shown in Fig. 7.6. The tune voltage is set to be 0 V for the phase noise measurement. At low offset frequency, the measured phase noise has a negative slope of 30 dBc/decade which is the $1/(\Delta f)^3$ dependant indicating $1/f$ noise is up-converted with other white noise from different noise sources in the circuit. As shown in Fig. 7.6, the phase noise increases after 10 hours RF stress compared to the fresh condition especially at low offset frequency. After high voltage stress, the flick noise of MOSFET is significantly increased due to hot-carrier degradation, especially for the n-channel transistor [80]. Flick noise is produced by traps at the SiO₂ and silicon interface. These traps can capture or reemit carriers from or to the channel, introducing flick noise in the drain current. The trap and release phenomenon occurs at low offset frequency more often and demonstrates a $1/f$ frequency dependence at low offset frequency. Hot-carrier induced traps are known to produce the same kind of noise from traps at the SiO₂ and silicon interface [81]. Hot carrier degradation significantly increases the $1/f$ noise of the MOSFET and thus increases the phase noise of the VCO under large-signal RF excitation.

7.3 Conclusion

A differential Clapp-VCO has been designed and successfully implemented in the TSMC 0.13 μ m CMOS process. Circuit is simulated and probed to examine the hot electron injection effect of the n-channel transistor in the Clapp-VCO. As seen in the simulation results, the negative transconductance transistors (M2 and M3) suffer more significant impact ionization under RF stress than the current source transistor M1. The oscillator's performances such as phase noise and tuned oscillation frequency before and after 10 hours of RF stress are measured

by experiments. The oscillation frequency increases after RF stress due to a decrease of the effective total capacitance after hot electron degradation. The measured phase noise increases after large-signal RF stress for 10 hours because the $1/f$ noise of the MOSFET increases significantly by hot electron degradation.

CHAPTER 8 : REALIABILITY OF A LOW PHASE NOISE CROSS-COUPLED LC VCO WITH P-CHANNEL TRANSISTORS

Phase noise is one of the most critical parameters for an oscillator. The low frequency noise of a pMOSFET is much lower than that of an nMOSFET which in turn is critical to reduce the close-in phase noise of a voltage controlled oscillator [82]. The VCO using pMOS transistors will have lower $1/f$ noise and potentially lower hot carrier induced white noise [83].

In this chapter, the design of a low-phase-noise differential cross-coupled LC-tank VCO with pMOS-core is presented. The oscillator performances regarding temperature effect, process variability are discussed.

8.1 Circuit Design

Fig. 8.1 shows the schematic of the designed differential Clapp-VCO with a cross-coupled pMOS pair which is the complimentary structure to the nMOS-core cross-coupled architecture. Transistors M1 and M2 are connected in differential configuration and are used to provide negative resistance to the oscillator to compensate for the loss in the LC tank. M3 is used as a current source. Here, the pMOS tail-current source is used since pMOSFET has lower $1/f$ noise than nMOSFET. The oscillation frequency is determined by the LC tank. The inductors are on-chip spiral inductors. The capacitors are implemented with inversion-mode pMOS varactors. The bulk of the pMOS device is connected to V_{DD} , the source and drain terminals of the pMOS are connected together and a tuning voltage is applied to tune the oscillation frequency. The gate of the pMOS varactors are connected to the drain of the cross-coupled differential pMOS pair.

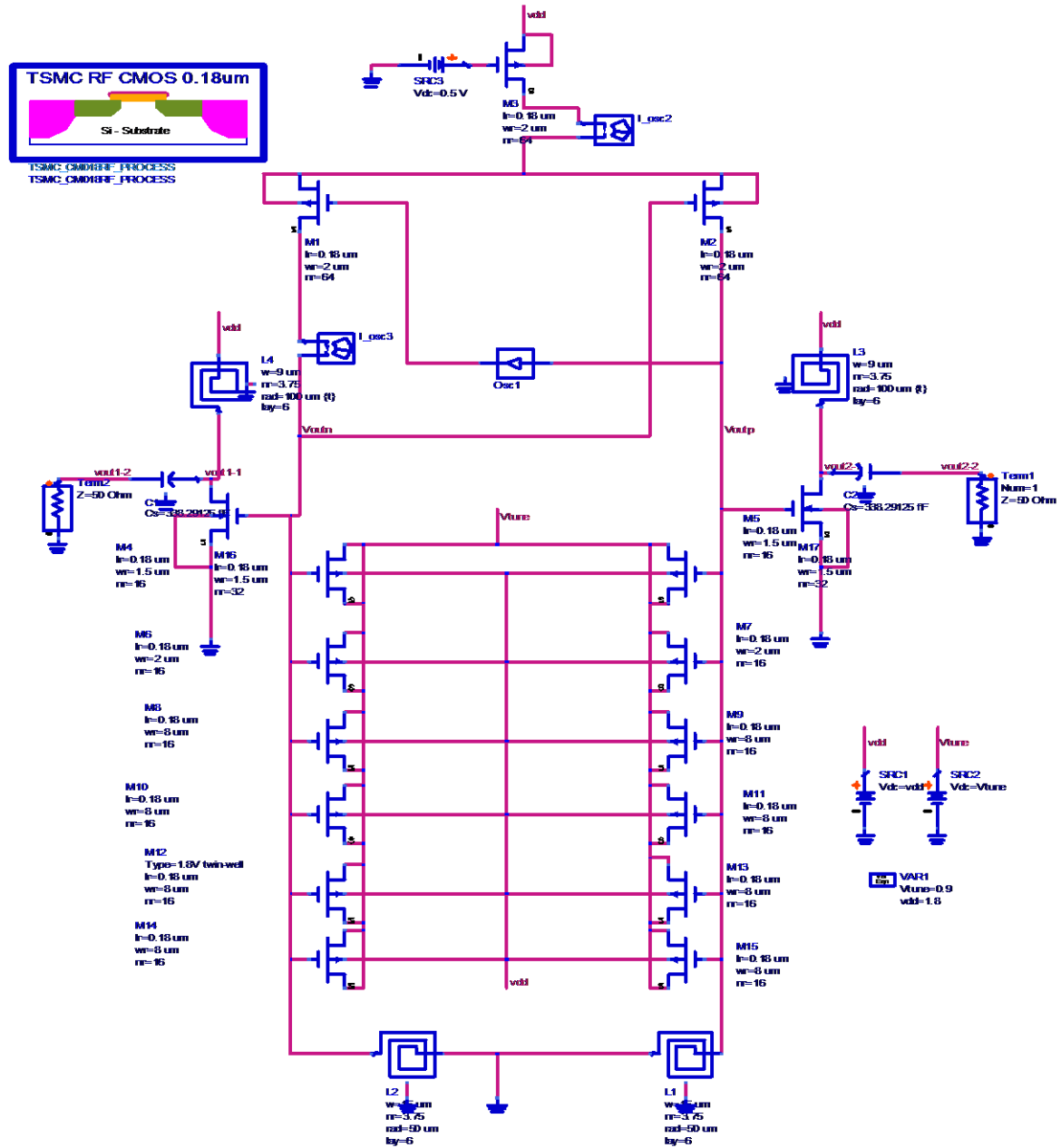


Figure 8.1 Schematic of the cross-coupled LC-tank VCO with p-channel transistors

Several pMOS varactors are connected in parallel to provide the desired capacitance. The capacitance value of the MOS capacitors depends on the voltage between bulk and gate. The MOS capacitors work only in depletion and inversion region providing monolithic change. The VCO is designed and implemented in the TSMC 0.18 μm 1P8M CMOS process. The supply voltage is 1.8 V.

The performances of the oscillator are simulated with ADS. Fig. 8.2 shows the phase noise as a function of offset frequency from the carrier at $V_{\text{tune}} = 0.9$ V. The phase noise is -125.184 dBc/Hz at 1 MHz offset frequency from the center frequency of 2.4038 GHz.

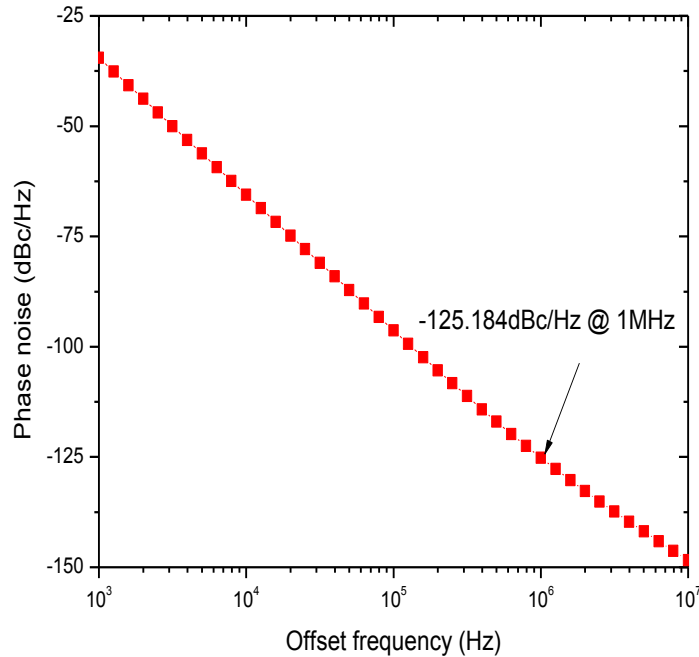


Figure 8.2 Phase noise versus offset frequency

Fig. 8.3 shows the tuning curve by varying the varactor's tuning voltage. The oscillation frequency varies from 2.3043 GHz to 2.5657 GHz as the tuning voltage sweeps from 0 V to 1.8 V, indicating a tuning range of 0.2614 GHz.

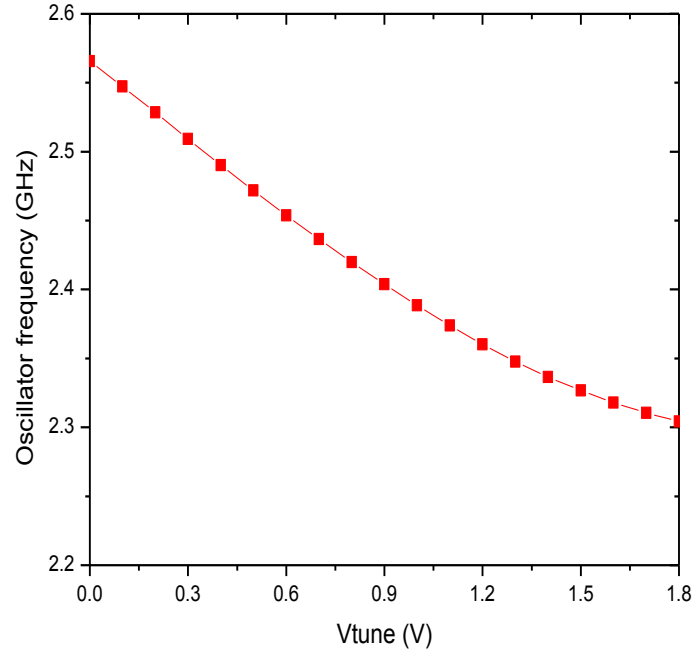


Figure 8.3 Tuning range

The layout of the oscillator is implemented using Cadence Virtuoso software with TSMC 0.18 μm layout library, followed by successful Calibre DRC for design rule checking and LVS for layout versus schematic verification. The layout of the circuit is shown in Fig. 8.4. Post-layout simulation is done in Agilent Advanced Design System (ADS) Momentum to get more accurate simulation results. Parasitic effects such as metal's impedance, capacitance between different metal layers and electrical and magnetic field effect and so on are extracted for all components and metal layers. The more accurate physical simulation results are obtained by composing these extracted parasitic effects with the ideal circuit

The simulation results of pre-layout simulation and post-layout simulation for the oscillator are shown in table 8.1. The phase noise at 1 MHz offset frequency from the carrier at $V_{\text{tune}} = 0.9$ V is -125.184 dBc/Hz for pre-layout simulation and is -125.704 dBc/Hz for post-layout

simulation with a difference of 0.52 dBc/Hz. The oscillation frequency at $V_{\text{tune}} = 0.9$ V is 2.321 GHz and 2.207 GHz for pre-layout simulation and post-layout simulation, respectively, with a difference of 0.114 GHz.

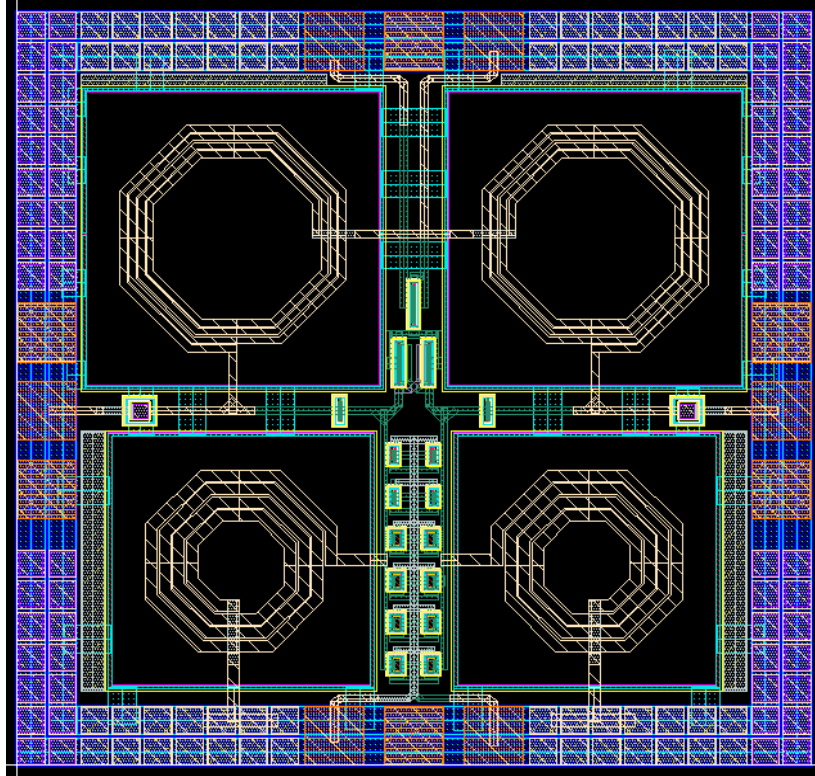


Figure 8.4 Chip layout

Table 8.1 Comparison of pre-layout simulation and post-layout simulation results

	Pre-layout simulation result	Post-layout simulation result
Phase noise at 1 MHz offset frequency ($V_{\text{tune}} = 0.9$ V)	-125.184 dBc/Hz	-125.704 dBc/Hz
Oscillation frequency at $V_{\text{tune}} = 0.9$ V	2.321 GHz	2.207 GHz
Tuning range	2.233 GHz ~ 2.459 GHz	2.134 GHz ~ 2.339 GHz

8.2 Reliability and Variability Discussion

8.2.1 The NBTI Effect

Degradation of pMOS transistors due to negative bias temperature stress is an important reliability concern in modern CMOS processes. Negative bias temperature instability leads to an increase of threshold voltage and decrease of the drive current due to the buildup of positive charges in gate oxide and surface states at Si-SiO₂ interface. Furthermore, the NBTI-generated interface traps and fixed charges are likely to increase $1/f$ noise, which is believed to be closely related to these charges [84]. Since the effect of NBTI is inversely proportional to gate-oxide thickness, the scaling of technology results in a significant increase in the susceptibility to NBTI degradation. The effect of negative bias temperature instability on the designed low-phase-noise cross-coupled LC-tank VCO with pMOS-core are examined here.

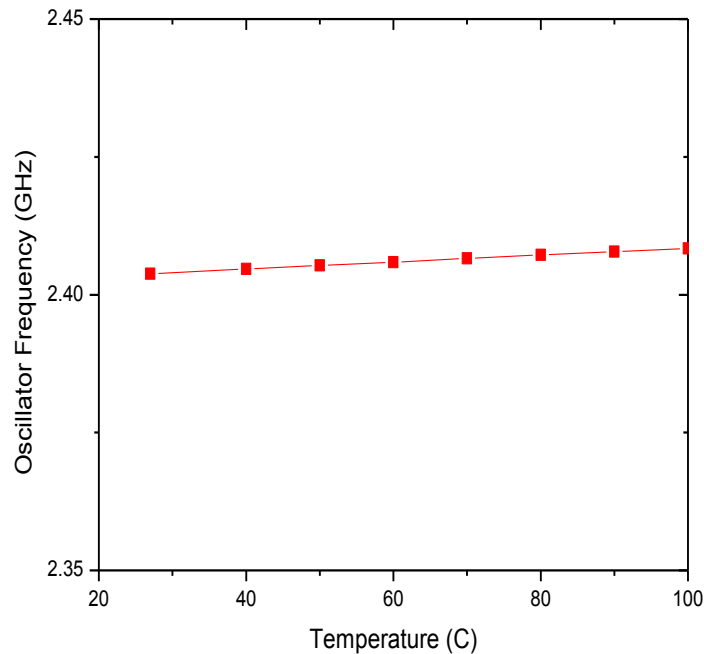


Figure 8.5 Temperature effect on oscillation frequency

The cross-coupled pMOS-core oscillator is simulated in Cadence Spectra by sweeping the temperature from 27 °C to 100 °C in simulation. The oscillation frequency as a function of temperature is shown in Fig. 8.5 with the tuning voltage set to be 0.9 V. The oscillation frequency almost keeps constant and is insensitive to the change of temperature.

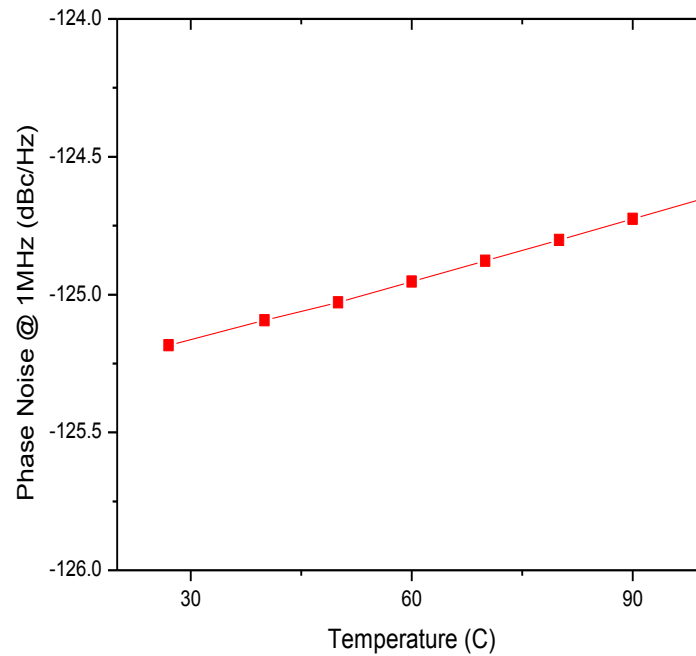


Figure 8.6 Phase noise at 1 MHz offset frequency versus temperature

Fig. 8.6 shows the phase noise at 1 MHz offset frequency from the carrier as a function of temperature at $V_{\text{tune}} = 0$ V. The phase noise at 1 MHz offset frequency from the carrier is -126.245 dBc/Hz at 27 °C and it is -124.746 dBc/Hz at 100 °C. Clearly, the phase noise increases at elevated temperature. At low offset frequency, $1/f$ noise is up-converted with other white noise from different noise sources. $1/f$ noise is related to the traps at the SiO_2 and silicon interface. The flick noise increases after NBTI effect since NBTI effect increases interface trapped charges

and fixed charges. Fig. 8.7 demonstrates the relationship of phase noise and the interface states. The default model used in the TSMC 0.18 μm library in Cadence for MOSFETs is the BSIM3 model. K_f is the flicker noise coefficient. K_f is chosen to be $4\text{e-}28$ to fit the default BSIM3 model for the fresh status. K_f increases from $4\text{e-}28$ to $2\text{e-}27$ to demonstrate the increase of interface state due to NBTI effect. As expected, the phase noise of the oscillator increases when K_f increases as shown in Fig. 8.7.

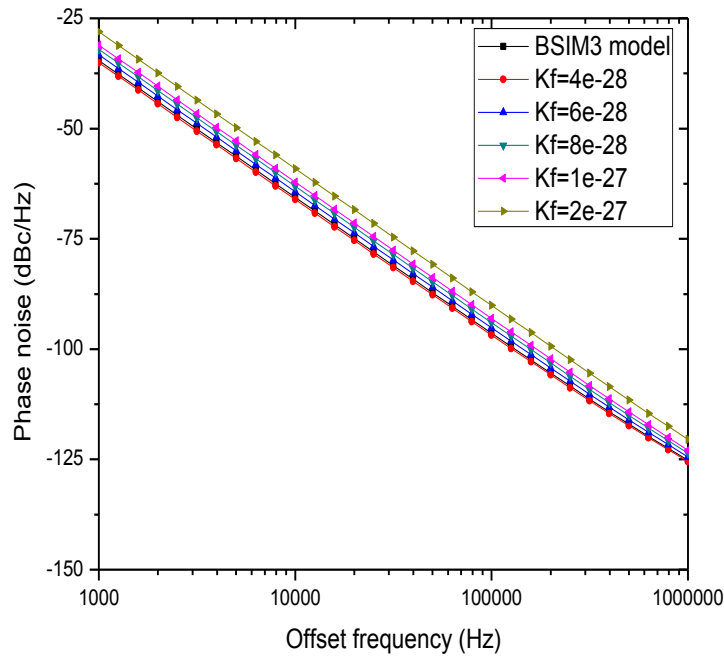


Figure 8.7 Phase noise versus offset frequency for different interface states

8.2.2 The Process Variability Effect

With the continued scaling of MOSFET devices, statistical process variations becomes one of the crucial issues in circuit designs using advanced CMOS technologies. Random dopant fluctuation, line-edge roughness, interface roughness, fixed charges and defects in dielectric can

cause threshold voltage shift, mobility variation and oxide thickness variation of MOSFET devices. This in turn results in significant performance variation on circuits. In this section, the performance variation of the cross-coupled LC-tank VCO with pMOS-core is investigated. Three different circuit configurations are compared for the robustness against process variations.

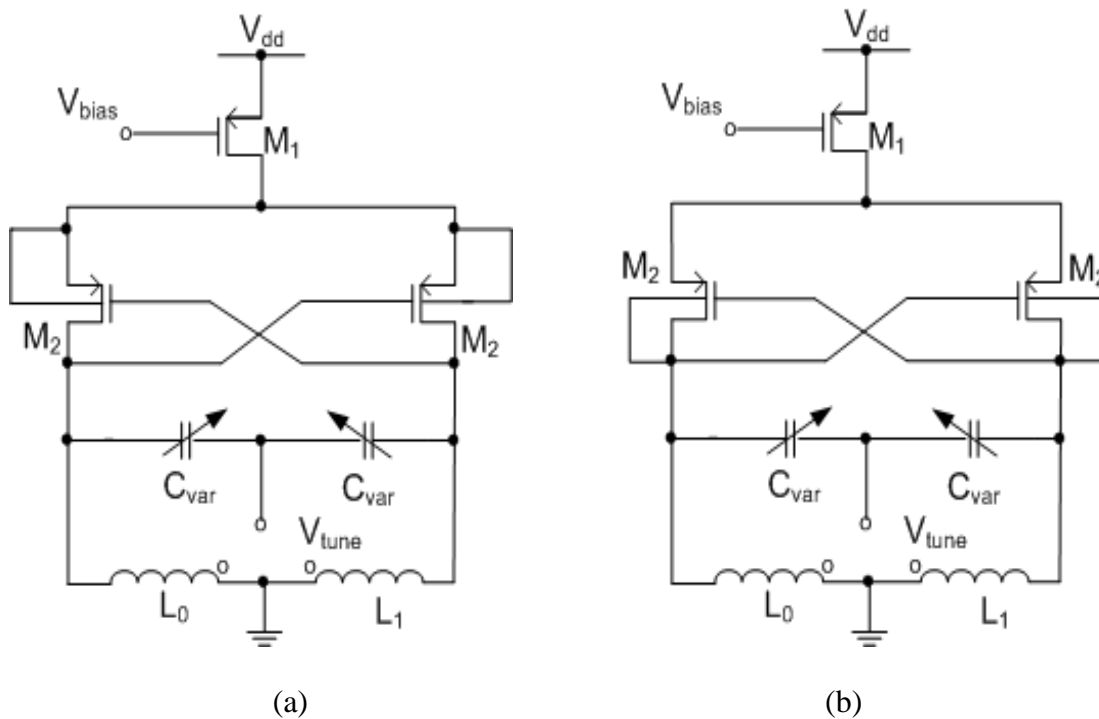
Table 8.2 shows the worst case corner models' value of the key parameters of the pMOSFET devices used in the circuit. Threshold voltage, mobility and oxide thickness are the major parameters affected by process variation. The worst case corner models are used to account for the windows of process variability. The value is extracted from the TSMC 0.18 μm model library in Cadence, where tt, ff, ss, fs, sf are represent typical model, fast-fast model, slow-slow model, fast-slow model and slow-fast model, separately.

Table 8.2 Key parameters value for the worst case corner models

	V_{th0} (V)	μ_0	$t_{ox}(\text{nm})$
tt_model	-0.449216	0.009795761	4.08
ff_model	-0.4254902	0.009851121	4.02740781
sf_model	-0.4254902	0.009851121	4.08
fs_model	-0.4729418	0.009740401	4.08
ss_model	-0.4729418	0.009740401	4.13259219

Three different circuit configurations for the cross-coupled LC-tank VCO with pMOS-core are shown in Fig. 8.8 (a)-(c). Fig. 8.8 (a) is the conventional connection where the body and the

source of the cross-coupled pMOS transistors M2 are tied together. Therefore, the source-body voltage of M2 is 0 V. There is no body effect exists and the threshold voltage of M2 keeps constant. Fig. 8.8(b) and (c) are two revised connections from Fig. 8.8 (a). In Fig. 8.8 (b), the body of the cross-coupled transistors M2 is connected to its drain. And in Fig 8.8 (c), the body of M2 is connected to its gate. The threshold voltage of the pMOS transistor with body effect can be expressed as: $V_{THP} = V_{THP0} + \gamma(\sqrt{|2\phi_{FP} + V_{SB}|} - \sqrt{|2\phi_{FP}|})$, where V_{THP0} is the threshold voltage when $V_{SB} = 0$, $\gamma = \sqrt{2q\epsilon_{si}N_{sub}/C_{ox}}$ is the body effect coefficient and V_{SB} is the source-bulk potential difference. For the circuits with the bulk of M2 connected to the gate or the drain, the bulk voltage is lower than the source voltage making $V_{SB} > 0$. The threshold voltage of the transistor is auto adjusted during the oscillation cycle.





To compare the robustness to process variations for the three different configurations, the three circuits are simulated in Cadence Spectra. Each circuit is simulated with the worst case corner models from TSMC 0.18 um model library in Cadence to get the performance variation from process variations. The tuning range and the phase noise are simulated and compared. Fig. 8.9 (a), 8.10 (a) and 8.11 (a) display the tuning range as a function of tuning voltage with different corner models for the circuits with body of M2 connected to source, drain and gate, separately. It's observed that the frequency variation induced from the corner models is largest for the circuit with body of M2 connected to the source and is smallest for the one with body of M2 connected to the gate. The phase noise as a function of offset frequency from the carrier with

different corner models at $V_{\text{tune}} = 0.9$ V for the circuits with body of M2 connected to source, drain and gate are shown in Fig. 8.9 (b), 8.10 (b) and 8.11 (b), separately. Same observation can be obtained that the phase noise variation due to the corner models is improved for circuits with body of M2 connected to drain and gate comparing to the circuit with body of M2 connected to source. The phase noise variation for circuit with body of M2 connected to gate is smallest.

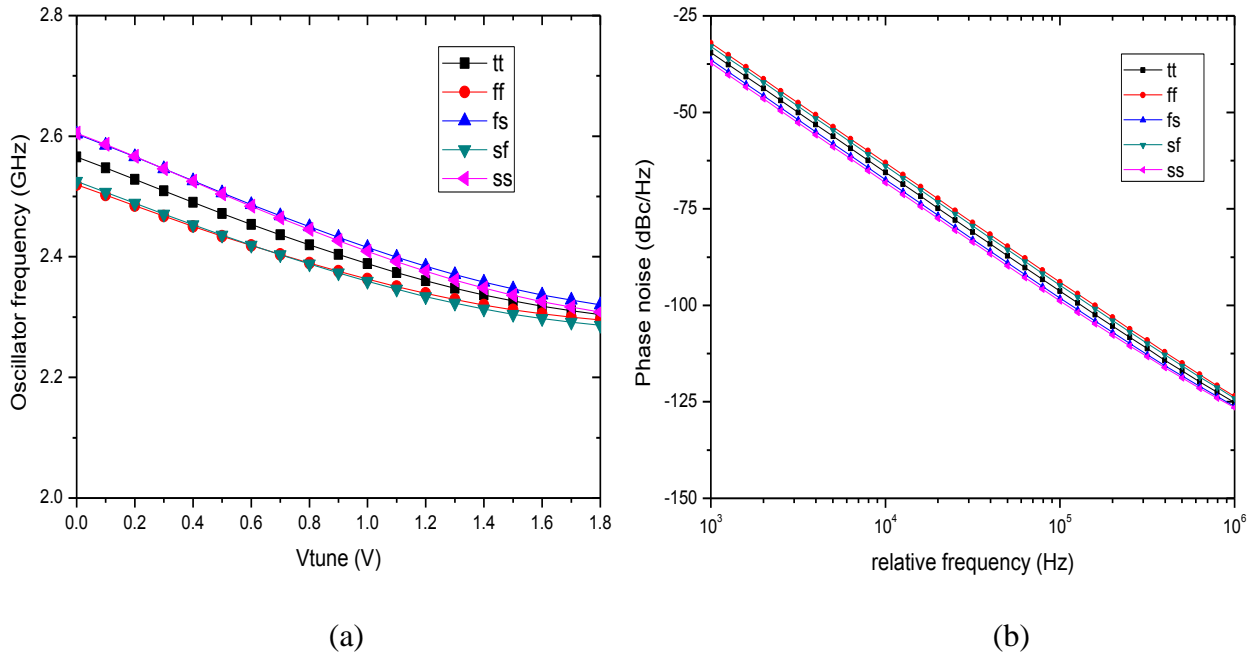


Figure 8.9 (a) Tuning range for different models (b) phase noise versus offset frequency for different models for traditional connection (V_B connected to V_S)

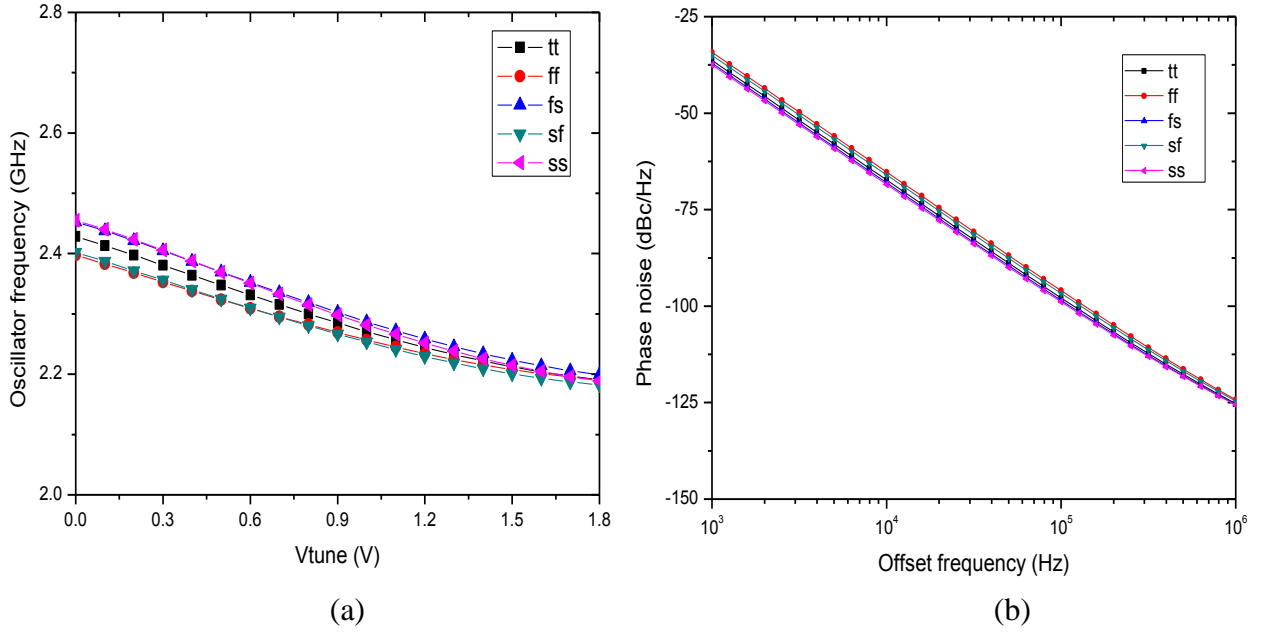


Figure 8.10 (a) Tuning range for different models (b) phase noise versus offset frequency for different models for revised connection 1 (V_B connected to V_D)

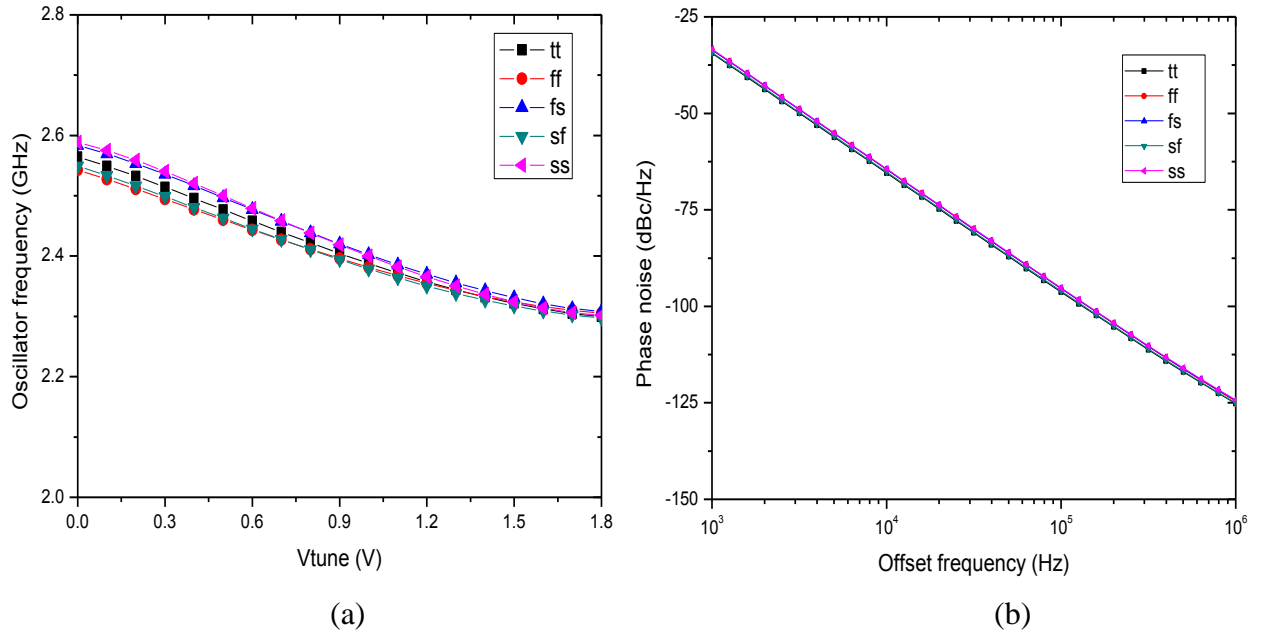


Figure 8.11 (a) Tuning range for different models (b) phase noise versus offset frequency for different models for revised connection 2 (V_B connected to V_G)

The comparison of oscillation frequency variation and phase noise variation to process variability for the three configurations is given in table 8.3. At $V_{\text{tune}} = 0.9 \text{ V}$, the oscillation frequency variation from process is 58.7 MHz for the circuit with body of M2 connected to source. For the circuit with body of M2 connected to drain, the oscillation frequency variation is 35.83 MHz while the oscillation frequency variation is 25.84 MHz for the circuit with body of M2 connected to gate. The phase noise variation at 1 MHz offset frequency from the carrier at $V_{\text{tune}} = 0.9 \text{ V}$ is 2.9 dBc/Hz for the circuit with body of M2 connected to source, 1.304 dBc/Hz for the circuit with body of M2 connected to drain and 0.939 dBc/Hz for the circuit with body of M2 connected to gate.

Table 8.3 Comparison of performance variation for three V_B configurations

	Unit	V_B to V_S	V_B to V_D	V_B to V_G
Oscillation frequency variation for different models @ $V_{\text{tune}} = 0.9 \text{ V}$	MHz	58.7	35.83	25.84
Phase noise variation for different models @ 1 MHz offset frequency @ $V_{\text{tune}} = 0.9 \text{ V}$	dBc/Hz	2.9	1.304	0.939

Fig. 8.12 to Fig. 8.14 demonstrate the Monte Carlo simulation results of the oscillation frequency and phase noise sensitivity subject to process variability for circuits with body of M2 connected to source, drain and gate, separately. The summary of Monte Carlo simulation results for the three configurations is shown in table 8.4. Monte Carlo simulation is done in Cadence with sample size of 1000. The oscillation frequency used to compare is at the $V_{\text{tune}} = 0.9 \text{ V}$. And the phase noise used to compare is at 1 MHz offset frequency from carrier with $V_{\text{tune}} = 0.9 \text{ V}$.

Monte Carlo simulation results demonstrate that for the oscillator with body of M2 connected to source has 0.75% oscillation frequency variation and 0.559 dBc/Hz spread for phase noise at 1 MHz offset frequency. The oscillator with body of M2 connected to gate has 0.628% oscillation frequency variation and 0.323 dBc/Hz spread for phase noise at 1 MHz offset frequency. And oscillator with body of M2 connected to drain has 0.503% oscillation frequency spread and 0.286 dBc/Hz spread for phase noise at 1MHz offset frequency. Comparing the plots of Fig. 8.12 to Fig. 8.14, it's apparent that the revised configurations with the body of M2 connected to drain and gate reduce the process variation effect than the original connection with the body M2 connected to its source.

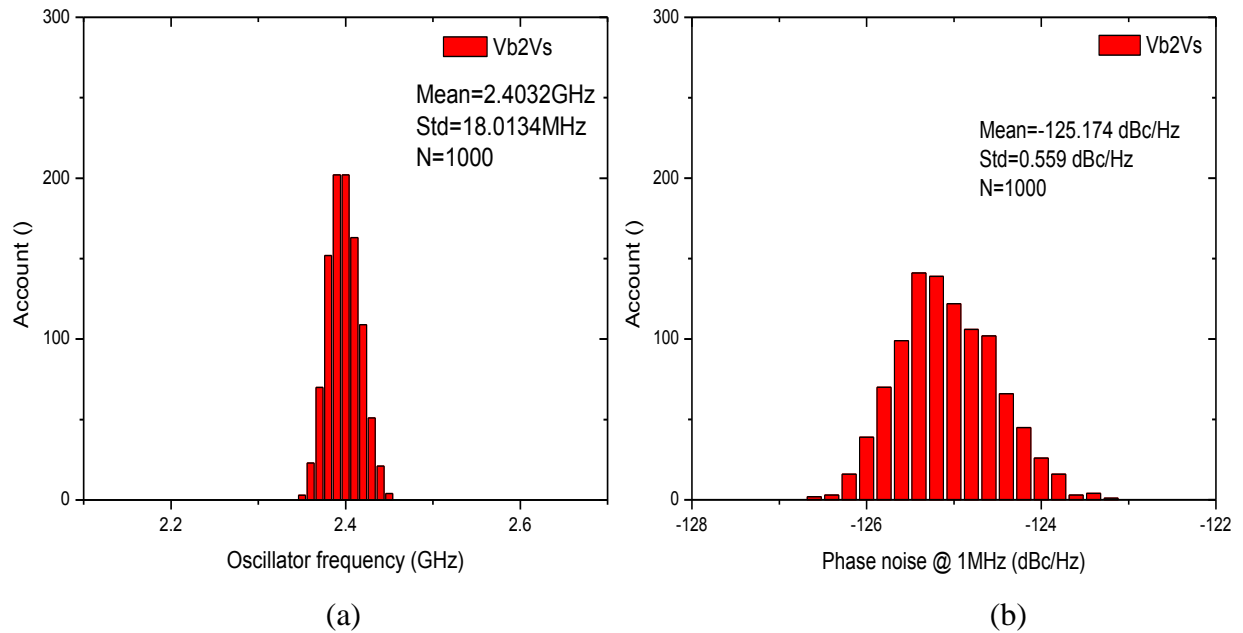


Figure 8.12 Monte Carlo simulation for traditional connection (V_B connected to V_S) (a) oscillation frequency (b) phase noise at 1 MHz offset frequency distribution

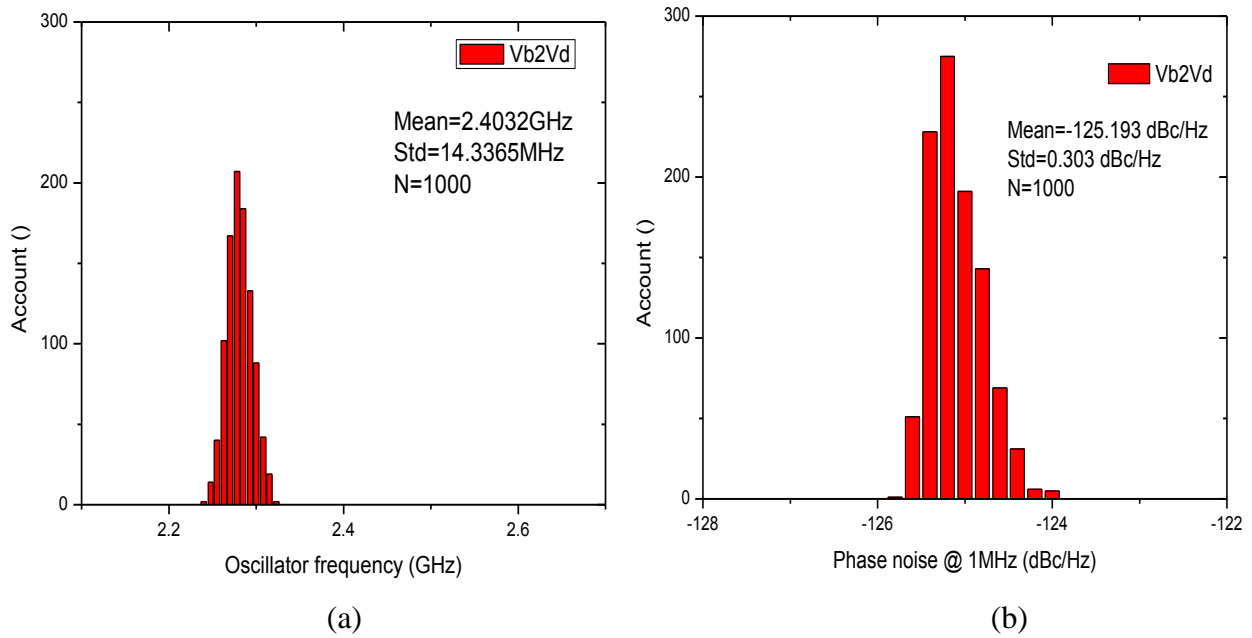


Figure 8.13 Monte Carlo simulation for revised connection 1 (V_B connected to V_D) (a) oscillation frequency (b) phase noise at 1 MHz offset frequency distribution

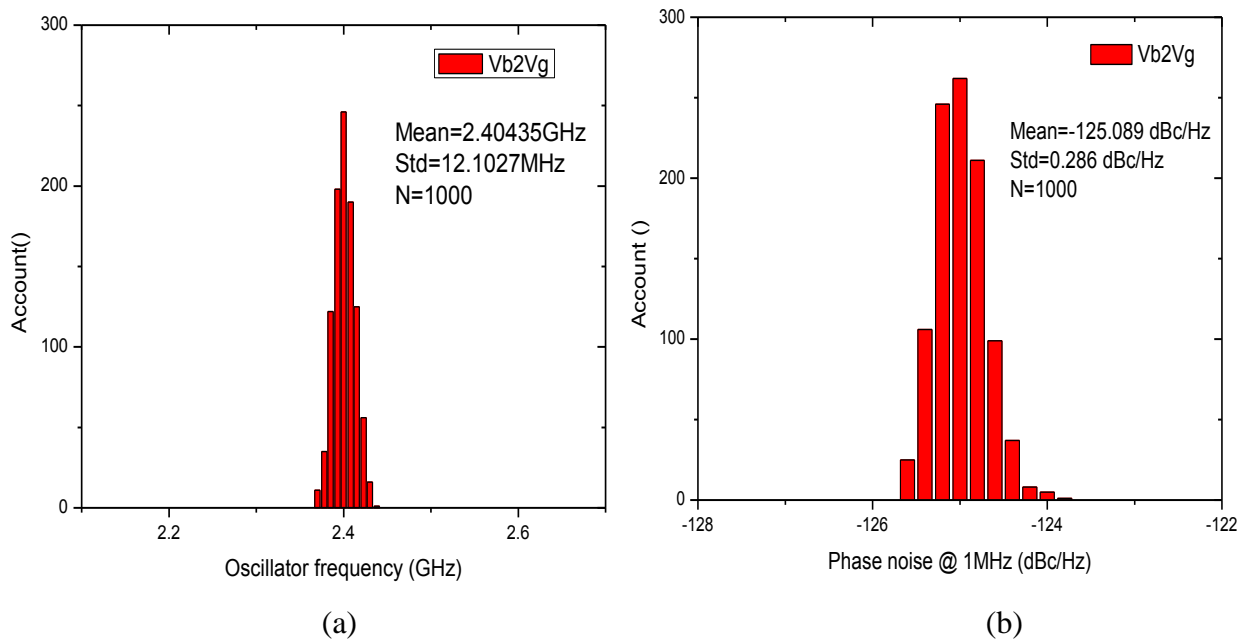


Figure 8.14 Monte Carlo simulation for revised connection 2 (V_B connected to V_G) (a) oscillation frequency (b) phase noise at 1 MHz offset frequency distribution

Table 8.4 Summary of Monte Carlo simulations for three V_B configurations

		Unit	V_B to V_S	V_B to V_D	V_B to V_G
Oscillation frequency	mean	GHz	2.4032	2.28455	2.40435
	std	MHz	18.0134	14.3365	12.1027
	%		0.750%	0.628%	0.503%
Phase noise @ 1 MHz offset frequency	mean	dBc/Hz	-125.174	-125.193	-125.089
	std	dBc/Hz	0.559	0.303	0.286
	%		0.447%	0.242%	0.229%

8.3 Conclusion

A cross-coupled LC-tank VCO with p-channel transistors is successfully designed in TSMC 0.18 μm CMOS technology. The transconductance transistors and the current source transistor are implemented with p-channel transistors for low phase noise since the p-channel transistors have smaller flicker noise than n-channel transistors. The oscillator performances such as oscillation frequency and phase noise subject to temperature effect are examined by simulations. The oscillation frequency is almost independent to the temperature based on the simulation results. The phase noise is degraded with the increase of the temperature. The NBTI effect at elevated temperature significantly increases the $1/f$ noise of the pMOSFET resulting in the increase of the phase noise of the VCO. Three different configurations of the body of the transconductance transistor connection are examined for the VCO against process variations. Worst corner model simulation and Monte Carlo simulation have been implored for oscillation

frequency and phase noise analysis. The VCOs with the body of the transconductance transistor connected to drain and gate are more resilient to process variations than the original configuration with the body of the transconductance transistor connected to its source.

CHAPTER 9 : CONCLUSIONS

The RF circuit design for device reliability degradations and process variations is proposed and investigated.

The adaptive gate-source biasing scheme is developed to improve the circuit reliability against device degradations. The adaptive method automatically adjusts the gate-source voltage to compensate the reduction in drain current subjected to various device reliability mechanisms. A class-AB RF power amplifier is used to validate the methodology. The use of a source inductance is more robust to reduce the variation of the third-order intercept point against device parametric degradations, while the use of a source resistance is more effective to maintain a stable power-added efficiency.

A RF power amplifier with an adaptive gate biasing is proposed to improve the circuit against device reliability degradations and process variations. The performances of the power amplifier with adaptive gate biasing are compared with those of the power amplifier without adaptive gate biasing technique. The adaptive gate biasing reduces PAE and output power sensitivity against device aging such as mobility and threshold voltage degradation. The adaptive gate biasing also makes the power amplifier more resilient to process variations as demonstrated by Monte Carlo simulation.

Injection locked voltage-controlled oscillators have been examined. The VCOs are implemented using TSMC 0.18 μm mixed-signal CMOS technology. Both the direct injection locked oscillator and the tail injection locked oscillator have improved phase noise performance than free running oscillators.

A differential clapp-VCO has been designed and successfully implemented in the TSMC 0.13 μm CMOS process for the evaluation of hot electron reliability. From the simulation results, the negative transconductance nMOS transistors suffer more significant impact ionization under RF stress than the current source transistor. The oscillator's performances such as phase noise and oscillation frequency before and after 10 hours of RF stress are measured by experiments. The oscillation frequency increases after RF stress due to a decrease in the effective total capacitance after hot electron degradation. The measured phase noise increases after large signal RF stress since the flick noise of the MOSFET increases significantly by hot-carrier degradation.

A cross-coupled LC-tank VCO with p-channel transistors has been designed for low phase noise. The simulation results show that the phase noise degrades after NBTI stress at elevated temperature. This is due to increased interface states after NBTI stress. The process variability has also been evaluated. The VCOs with the body of the transconductance transistor connected to drain and gate are more resilient to process variation than the original configuration with the body of the transconductance transistor connected to its source.

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